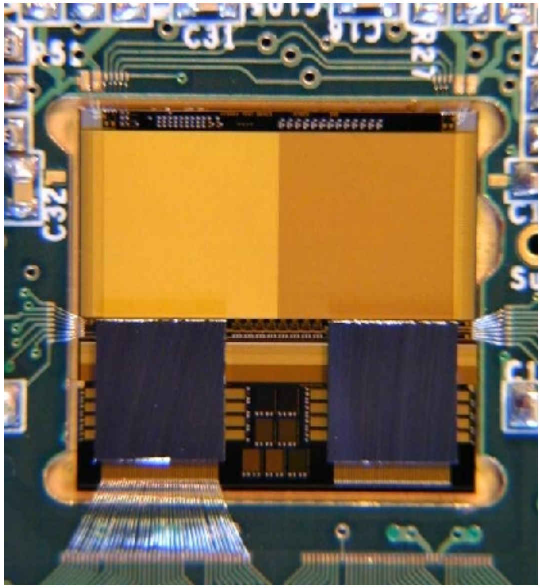
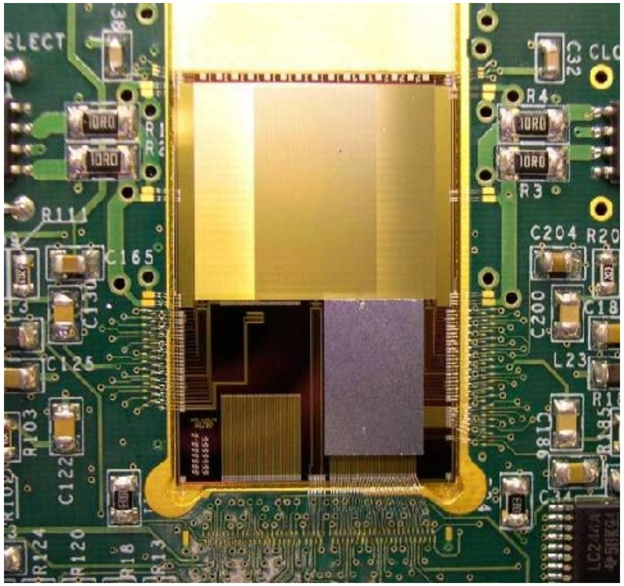
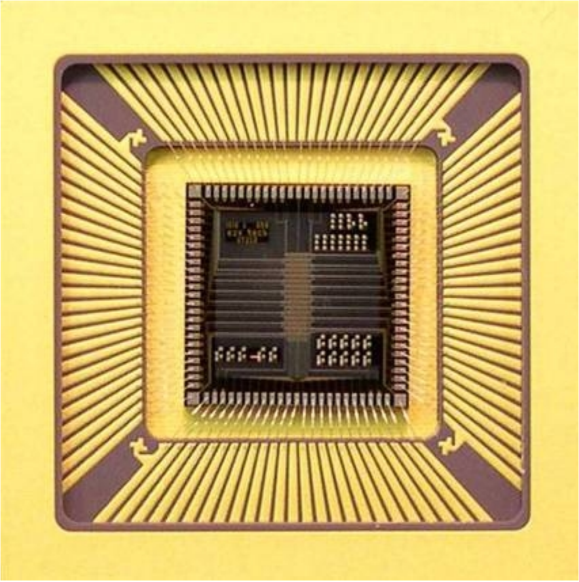
CCD-based Sensors for High Energy Physics

Konstantin Stefanov





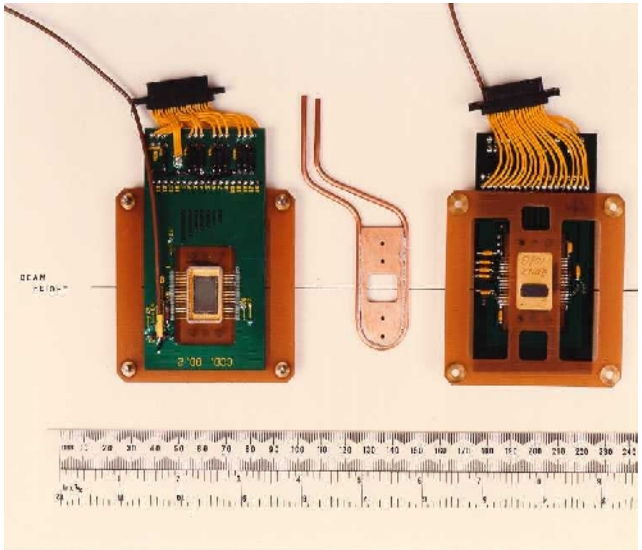


Short Personal Introduction

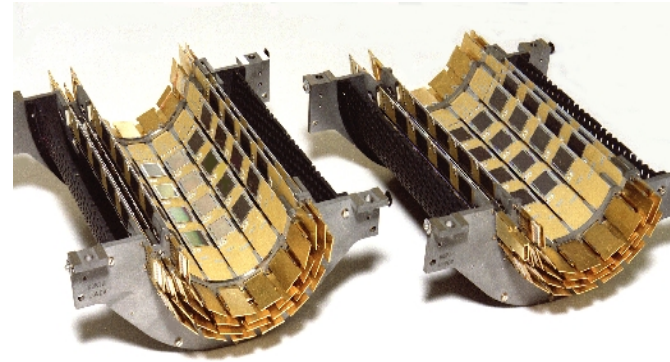
- PhD in physics from Saga University, Japan
  - Thesis on radiation damage effects in CCDs, caused by electron and neutron damage
  - CCDs were intended for use in a vertex detector
  - Particle tracking to micron level in high energy physics experiments
- Worked at Rutherford Appleton Laboratory (UK) for 7 years
  - Development of CCD-based sensors for the vertex detector at the International Linear Collider
  - High speed column parallel CCDs
  - Novel "CCD in CMOS" devices
- Presently at Sentec Ltd, Cambridge, England
  - Scientific and electronics consultancy company

Contents

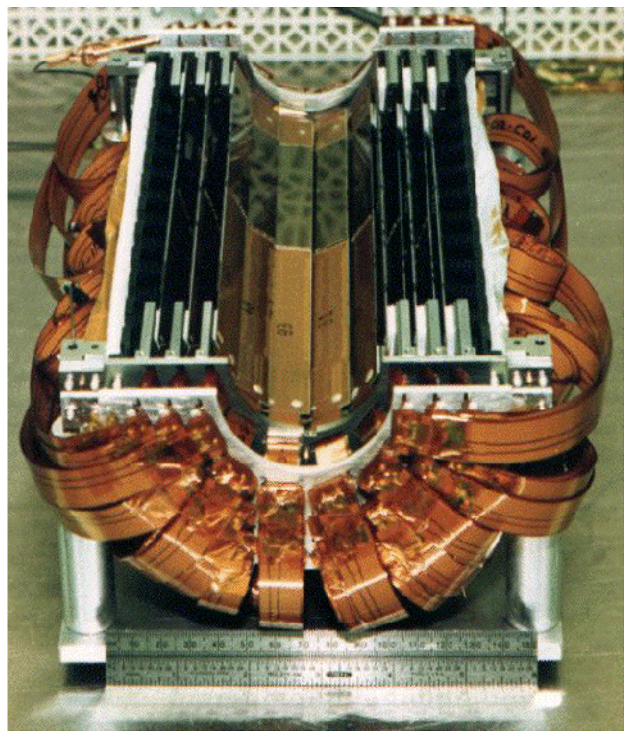
- CCD principles
- High speed column parallel CCDs
- CCD-based in-situ storage image sensor (ISIS) in CCD and CMOS technologies
- Future very large scale pixel detectors – Silicon Pixel Tracker



The first CCDs used for studies of charm production at CERN (NA32 experiment, 1984)

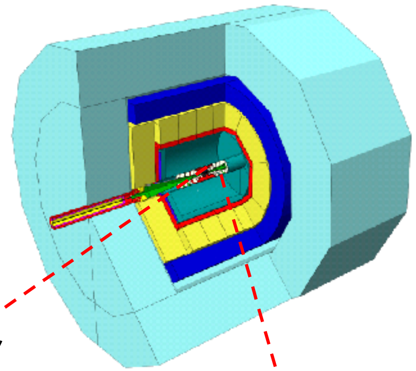


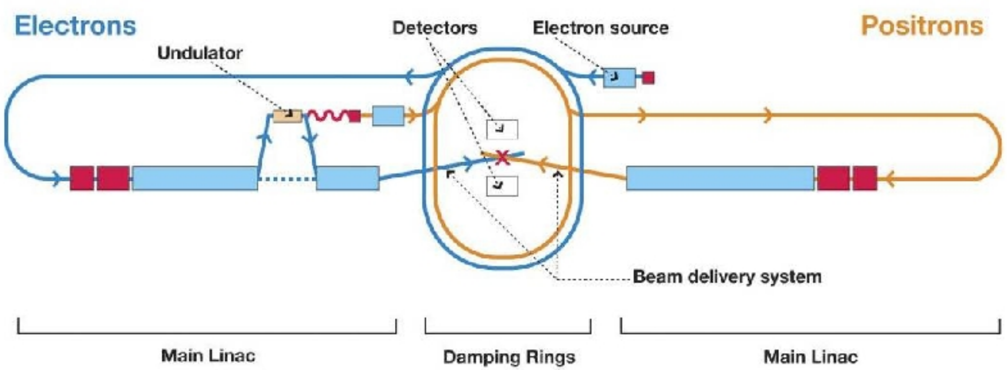
The VXD2 vertex detector at the Stanford Linear Collider (1992)



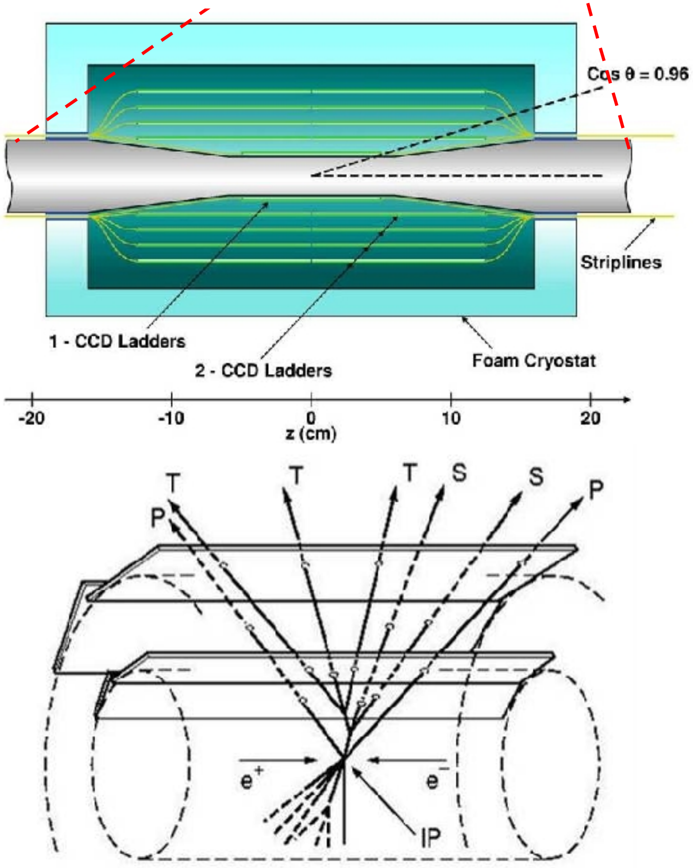
The VXD3 upgrade vertex detector: 96 large CCDs, 307 Million pixels (1996)

Vertex Detector for the International Linear Collider (ILC)

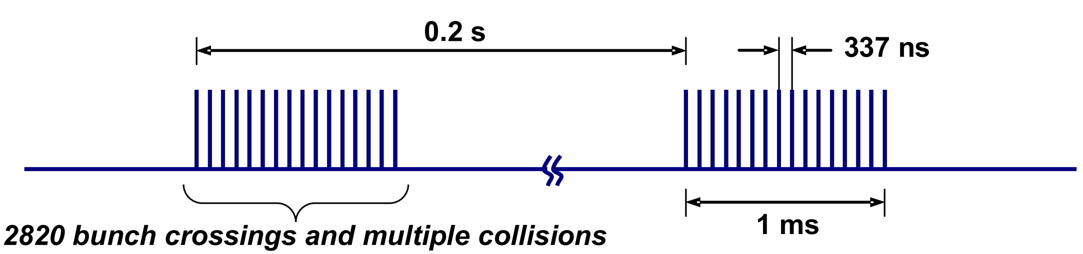




Vertex detector



- The vertex detector is nearest to the beam pipe - "tracking microscope"
- Contains almost a billion pixels (20 μm × 20 μm)
- Beam timing, power and material constraints make the development very challenging
- CCD-based detector development at RAL focused on the ILC requirements



CCDs as Particle Detectors

Numerous advantages:

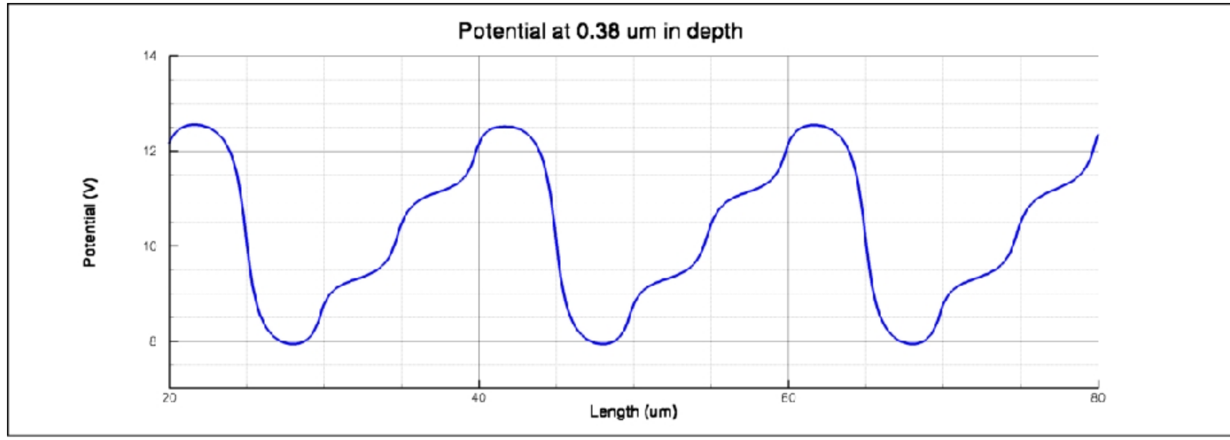
- Small pixel size – 20 μm for ILC, but down to below 3 μm possible;
- Thin sensitive volume – e.g. 20 μm epitaxial layer, signal is ≈80 e-/μm of track;
- Good spatial resolution helped by charge spreading;
- 100% fill factor – Full Frame Transfer CCDs;
- Excellent uniformity in response and gain;
- Low readout noise : below 10 e- at 1 MHz;
- Large, wafer-scale devices available

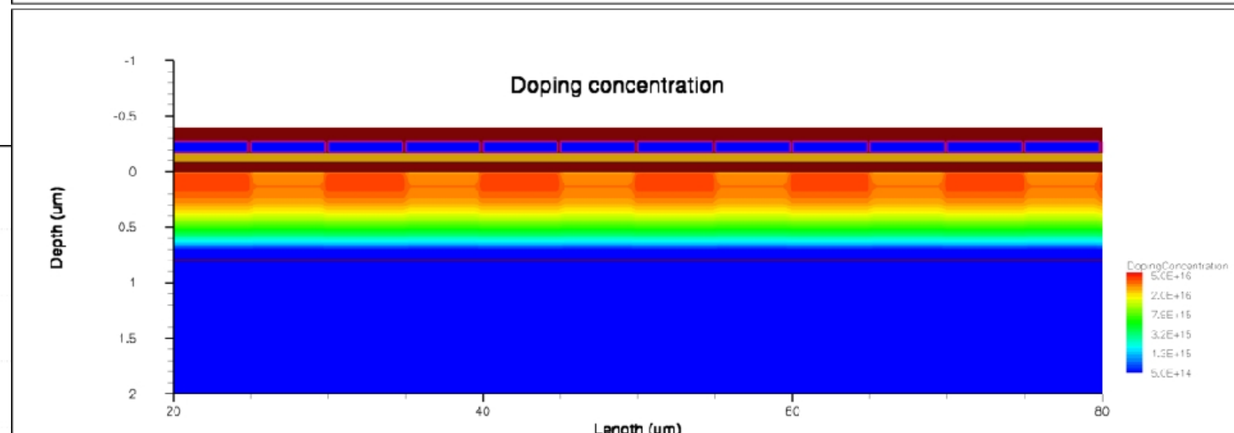
However …

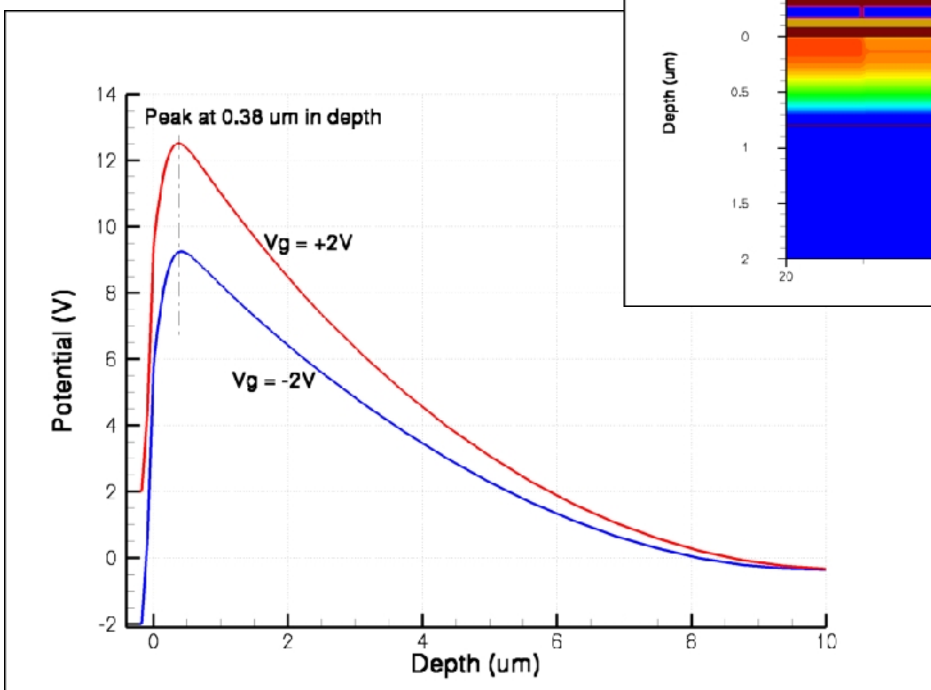
- Vulnerable to bulk radiation damage effects – Charge Transfer Inefficiency
- Power dissipation in the output source followers is high, lots of bias voltages
- Difficult to integrate with CMOS logic on the same chip
- Image area has large capacitance, challenge to drive at high speeds

Buried Channel CCD:

- Starting material is *p*-type epitaxial layer
- *n*-type implant creates potential peak at depth of ~100 nm
- Charge is kept away from traps at the surface





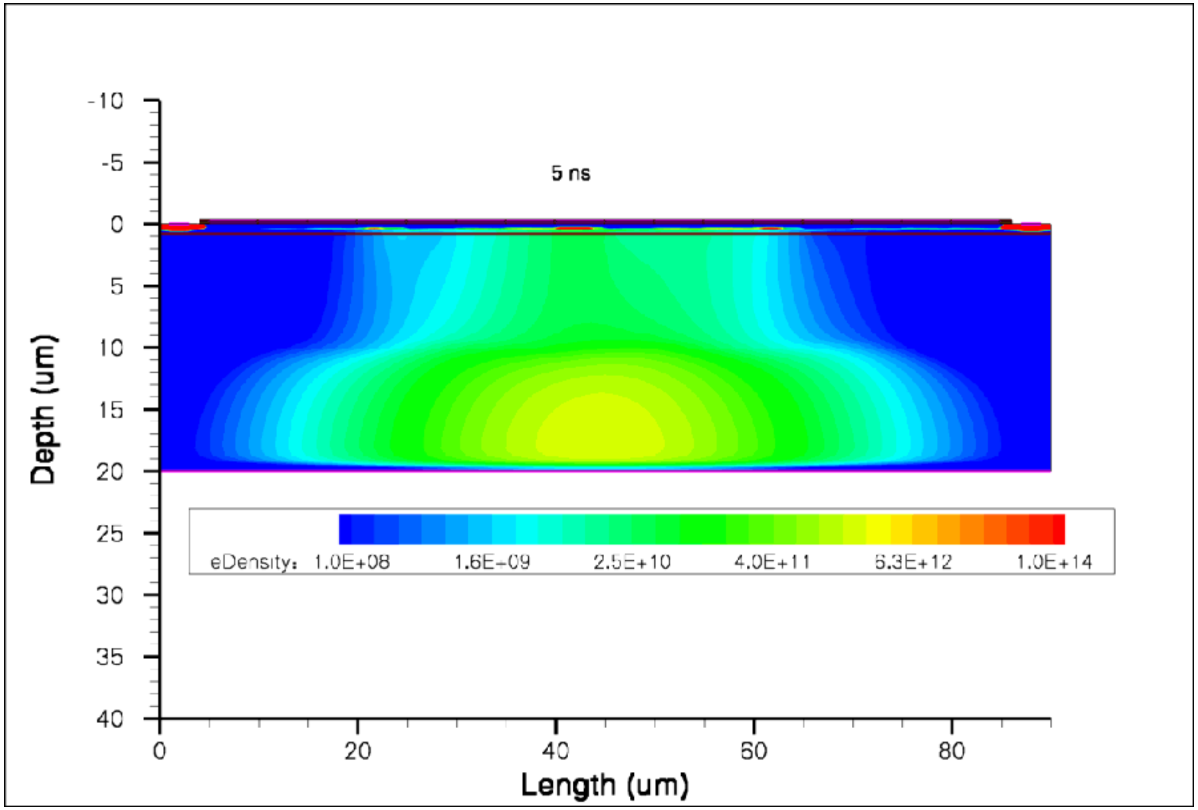


Two-phase CCD:

- Additional *p*-type inter-gate implant creates potential barriers for charge separation
- Symmetry of drive

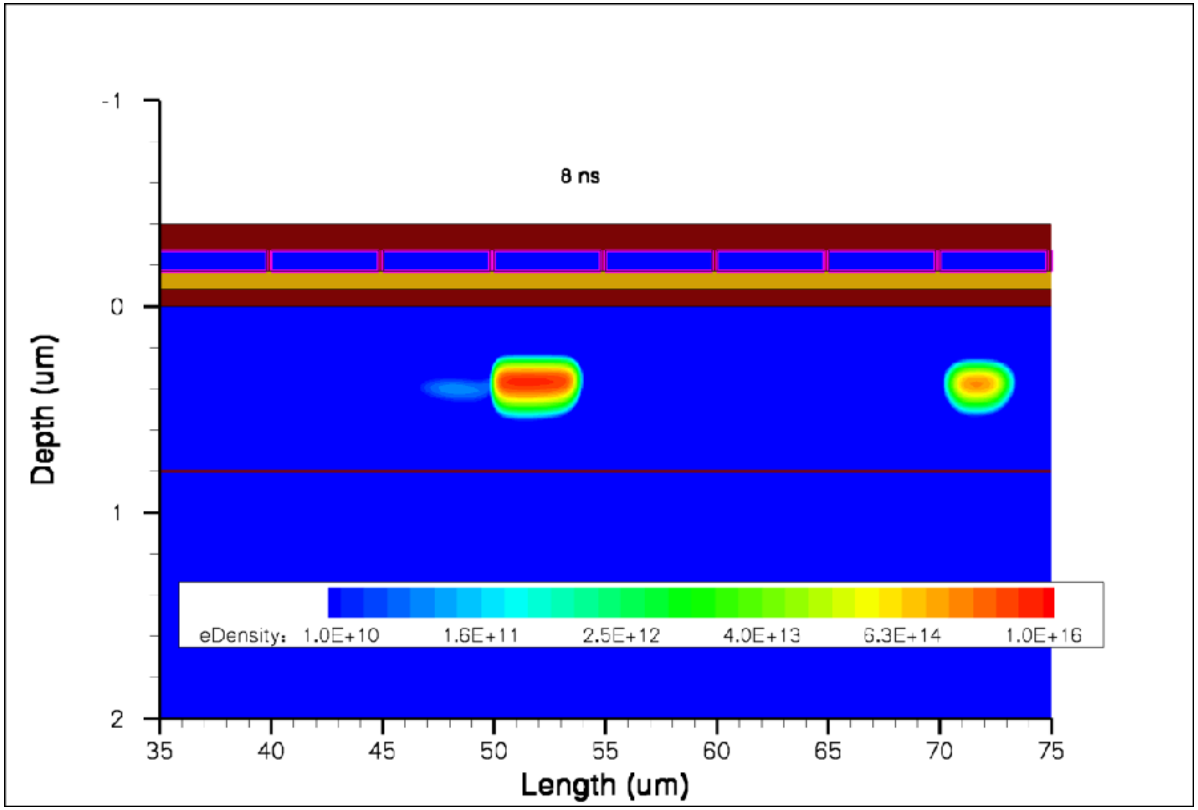
Charge Collection in CCDs

- Two-phase buried channel CCD with 20 µm thick, 100 Ω.cm epitaxial silicon;
- Pixel size: 20 µm
- About 10 µm is depleted

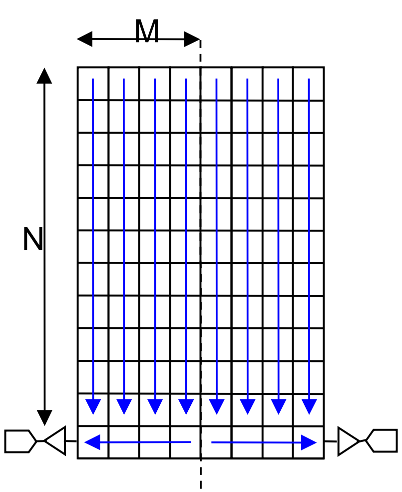


Charge Transport in CCDs

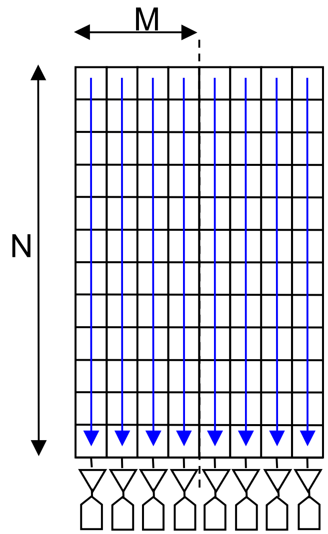
- Two-phase CCD
- Clocks change from -2 V to +2 V (and from +2 V to -2 V) in 10 ns



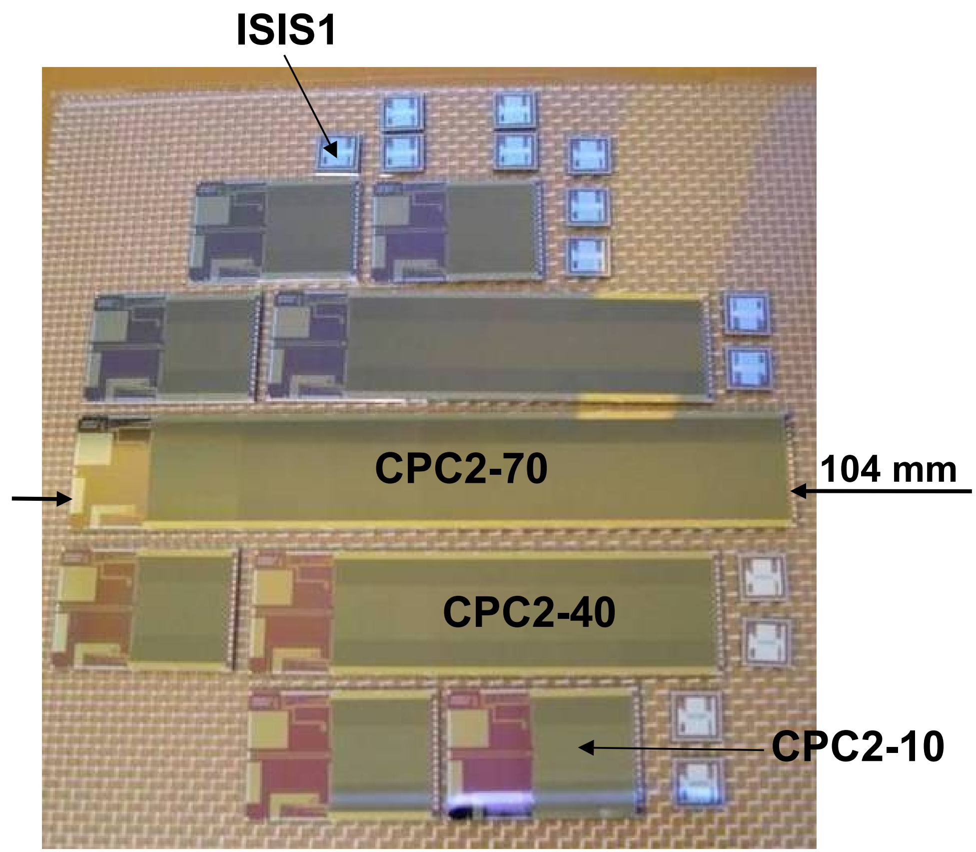
The Column Parallel CCD (CPCCD)



“Classic CCD”
Readout time ≈ $N \times M/f_{out}$



Column Parallel CCD
Readout time = N/f_{out}

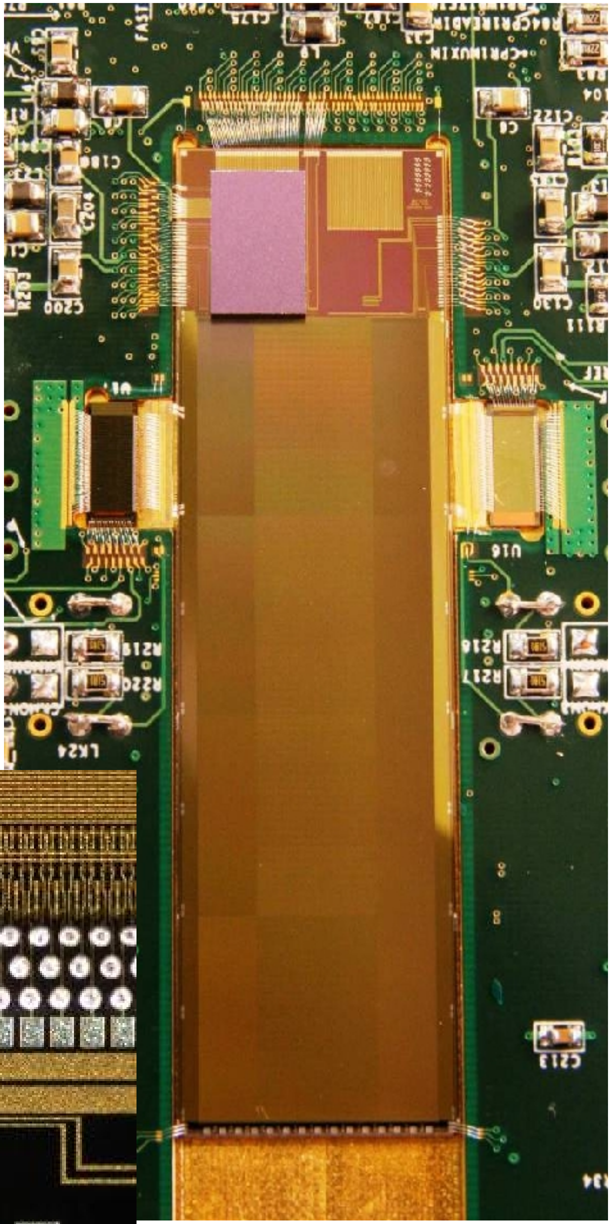


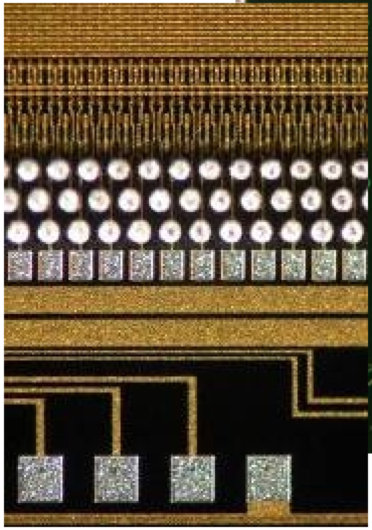
CCDs made by e2v Technologies

- **The CPCCD is an extremely fast type of CCD employing massive parallel readout**
- **Two generations of CPCCDs produced to date**
- **Clock amplitude is only 1.4 V_{pkpk} sine wave, noise < 75e- @ 10 MHz**

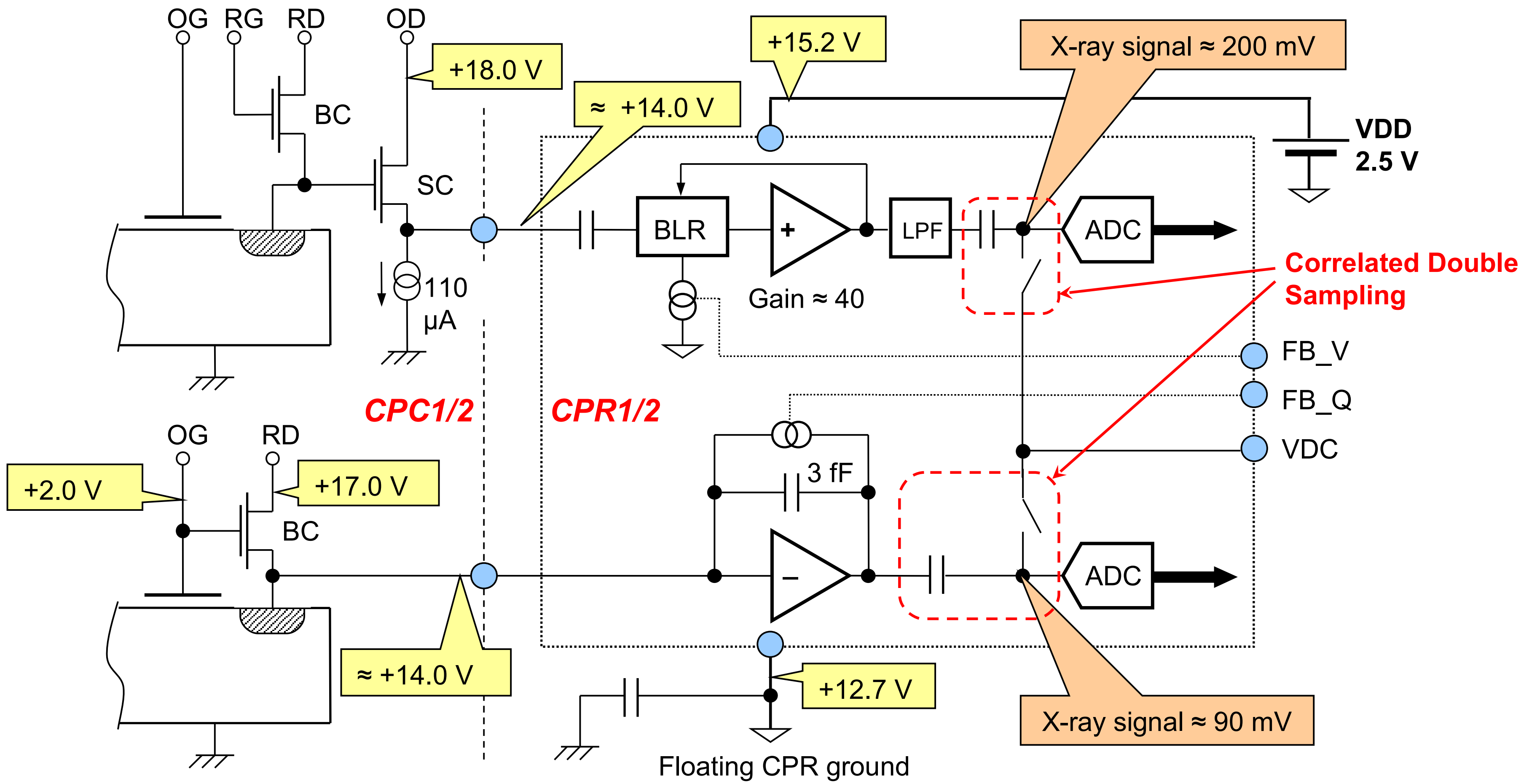
Bump-bonded CPCCD with Readout ASIC

- Dedicated readout and driver ASICs developed at RAL
  - Readout chip employs sparse data algorithms
  - Driver delivers CCD clocks up to 20 Amps at 50 MHz
- Bump-bonded CPC2-40/CPR2 driven by two CPD1 chips
  - First time e2V CCDs have been bump bonded
  - Works up to 9 MHz (standalone CCD up 45 MHz)
  - 5 cm long CCD, signals pass 5 “stitches”
  - Performance of the readout chip is limiting factor, and gradually deteriorates at higher frequencies (missing and/or spurious codes)

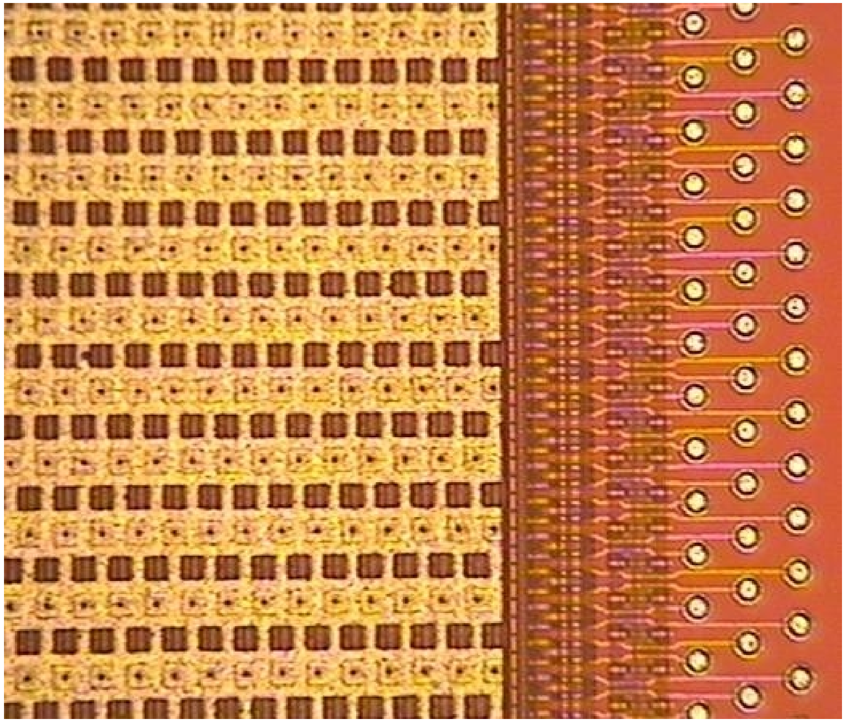




How the CPC and the CPR Work Together



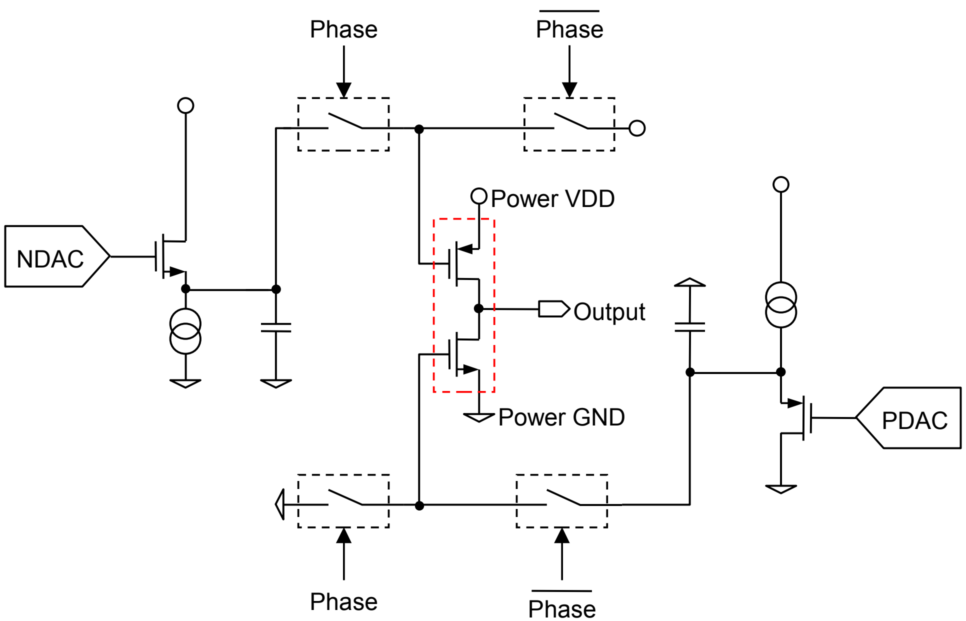
Busline-free CPCCD

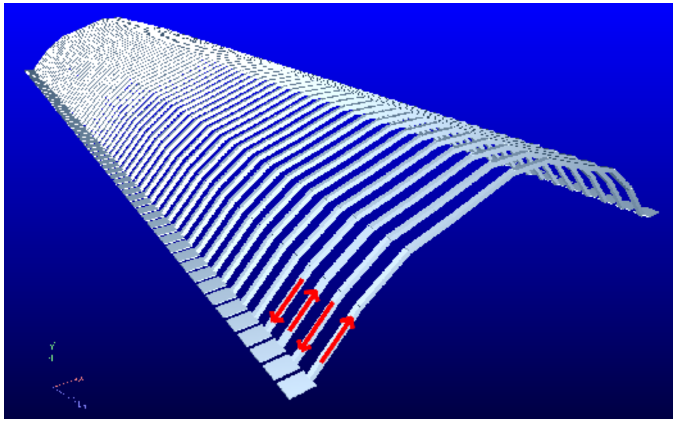


- One of the major problems with the CPCCD is the driving of the huge gate capacitance (e.g. 40 nF at 50 MHz sine wave)
  - Low clock amplitudes essential, below 2 Vpp
  - Traditional clock distribution (busline along the chip edge) does not work
- High speed (busline-free) devices with 2-level metal clock distribution:
  - The whole image area serves as a distributed busline
  - Special technique developed to work with the single level metal at e2V

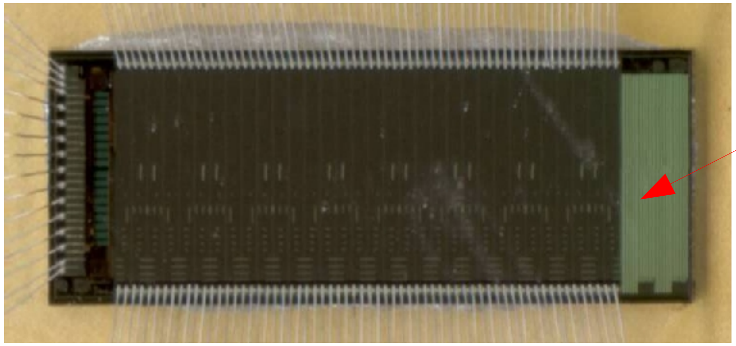
Clock Driver for CPC2: CPD1

- Designed to drive:
  - Outer layer CCDs (127 nF/phase) at 25 MHz
  - Layer1 CCDs (40 nF/phase) at 50 MHz
  - CPC2 requires 21 Amps/phase @ 2V$_{pkpk}$
- One chip drives 2 phases, up to 3.3 V clock swing
- 0.35 μm CMOS process, chip size 3 × 8 mm²
- 8 independent clock sections
- Careful layout on- and off-chip to cancel inductance, bump-bondable
- Parasitic inductance kept in the order ~100 pH (stand-alone bond wire is 1 nH/mm!)



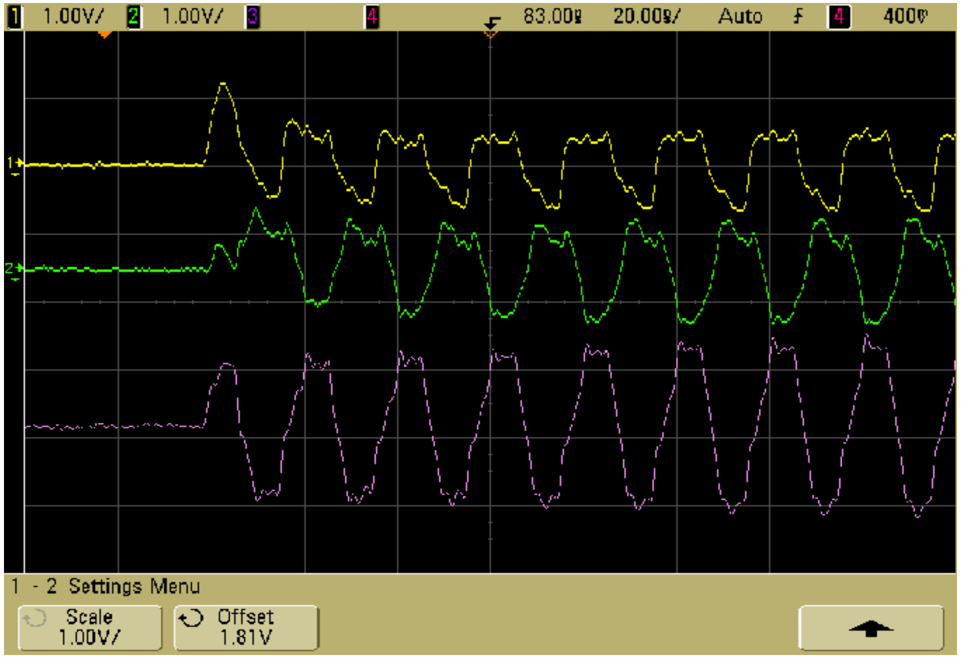


Clock Driver for CPC2 : CPD1



Steve Thomas, Peter Murray, RAL

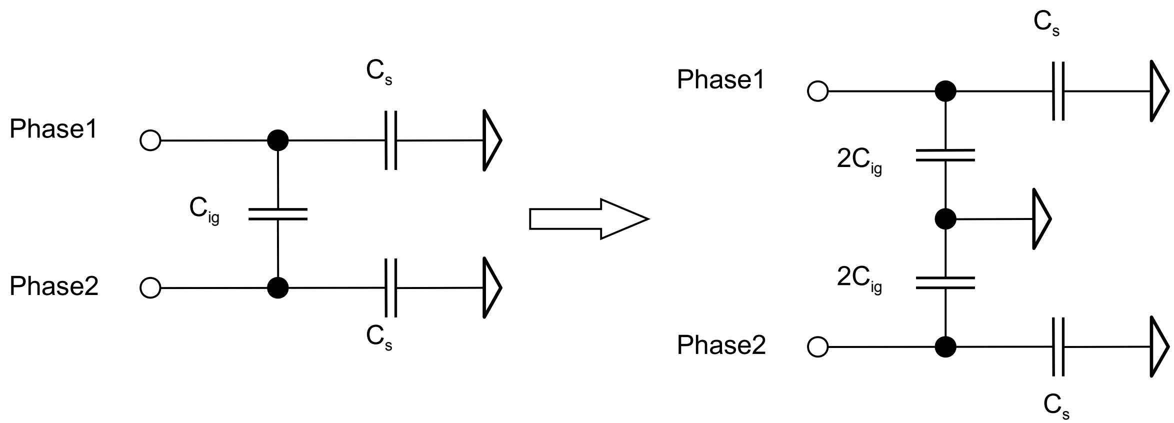
- Internal 2 nF load capacitor to one section
- CPD1 driving 32 nF-equivalent internal load at 50 MHz



2 $V_{pk\text{-}pk}$ differential clocks

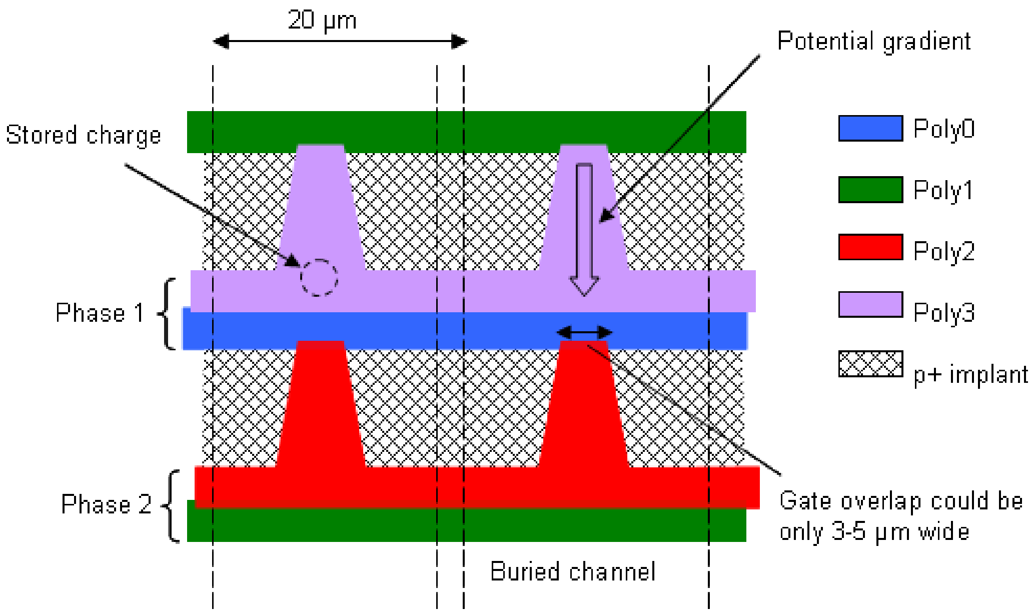
Rui Gao, Andrei Nomerotski, Oxford U

CCDs for Lower Gate Capacitance

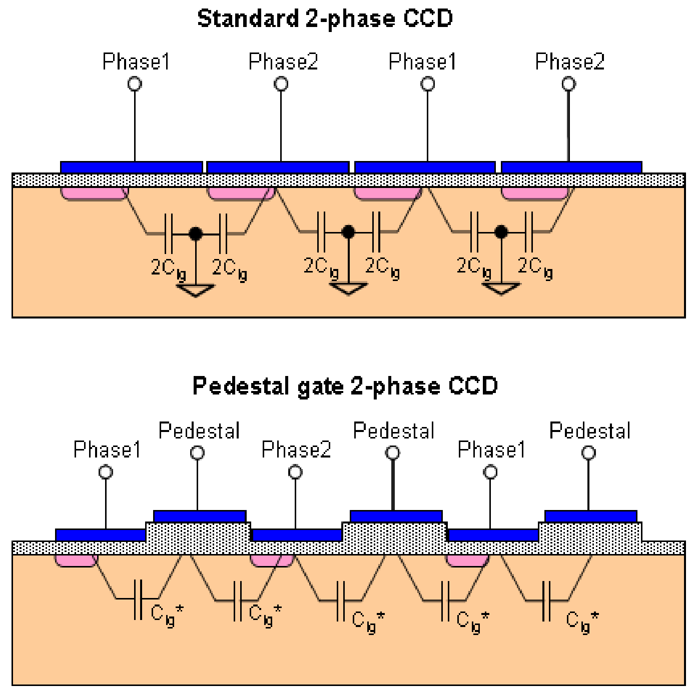


- **High CCD capacitance is a challenge to drive because of the currents involved**
  - ❖ **Can we reduce the capacitance and the clock amplitude? *(both reduce power)***
  - ❖ **Inter-gate capacitance C_{ig} is dominant, depends mostly on the size of the gaps and the gate area**
  - ❖ **New ideas for reduced overlap promise to reduce C_{ig} by a factor of up to 4.**
- **Together with e2V Technologies designed several small CCDs to test ideas for reduction of capacitance and clock amplitude.**

CCDs for Lower Gate Capacitance



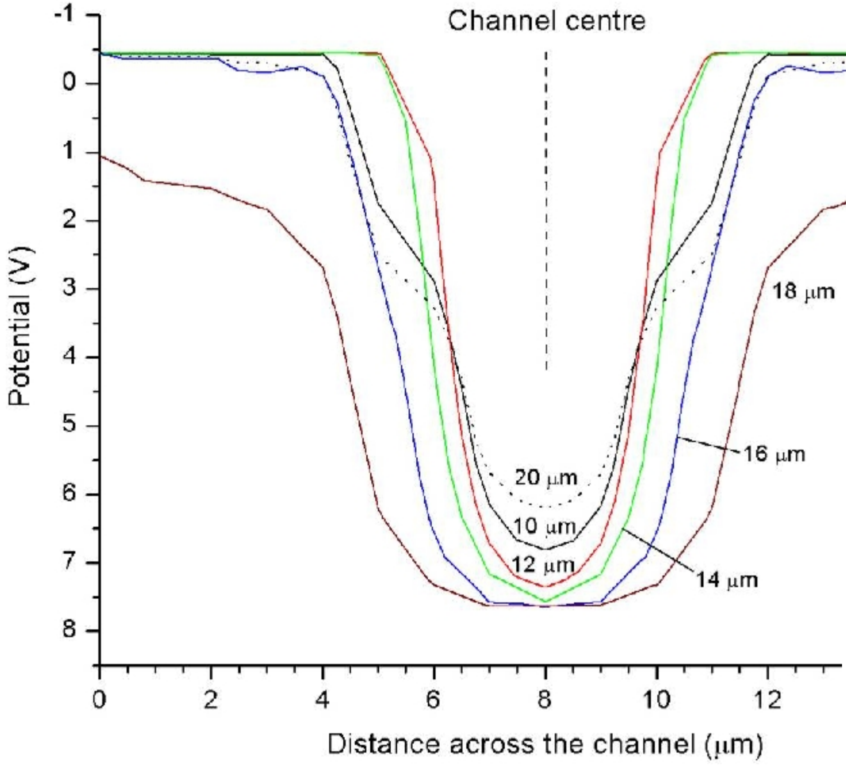
Open gate CCD

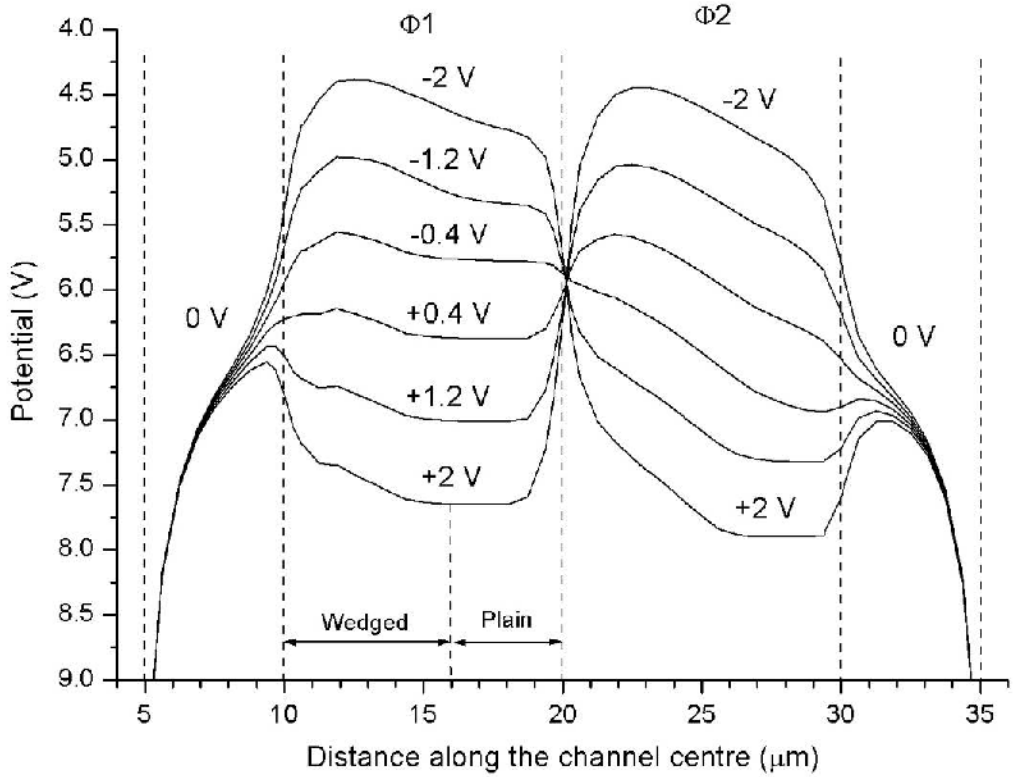


"Pedestal gate" CCD

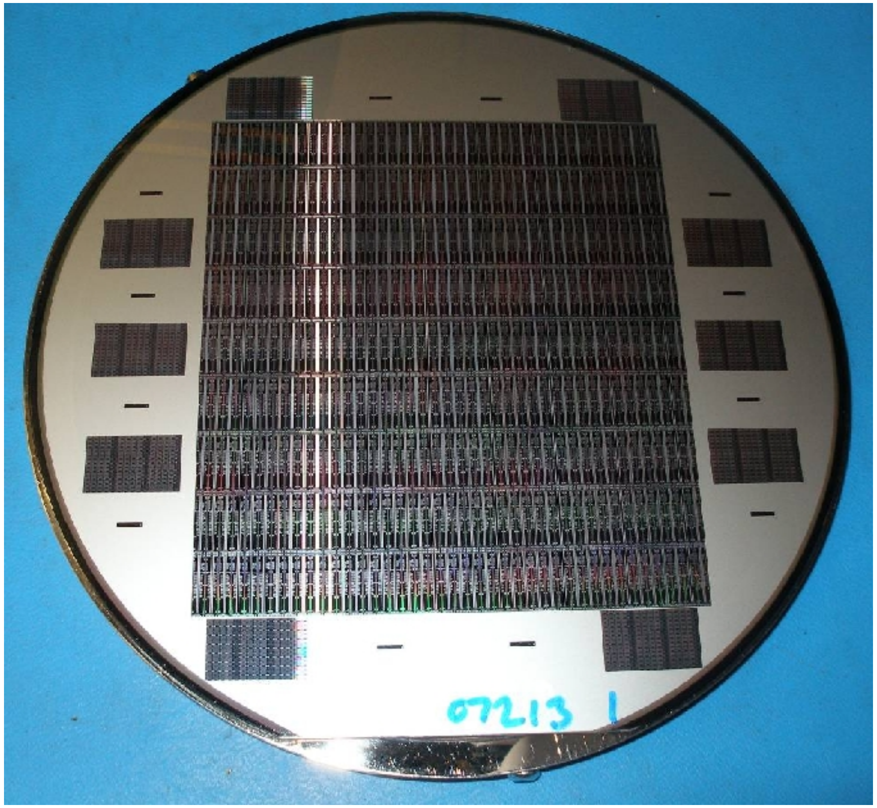
- Inter-gate capacitance C_{ig} is dominant
- C_{ig} depends mostly on the size of the gaps and the gate area
- Open phase CCD – profiled gates, could reduce C_{ig} by a factor of 2.
- "Pedestal gate" CCD – promises to reduce C_{ig} by a factor of 4.

Open Phase CCD with Channel Taper



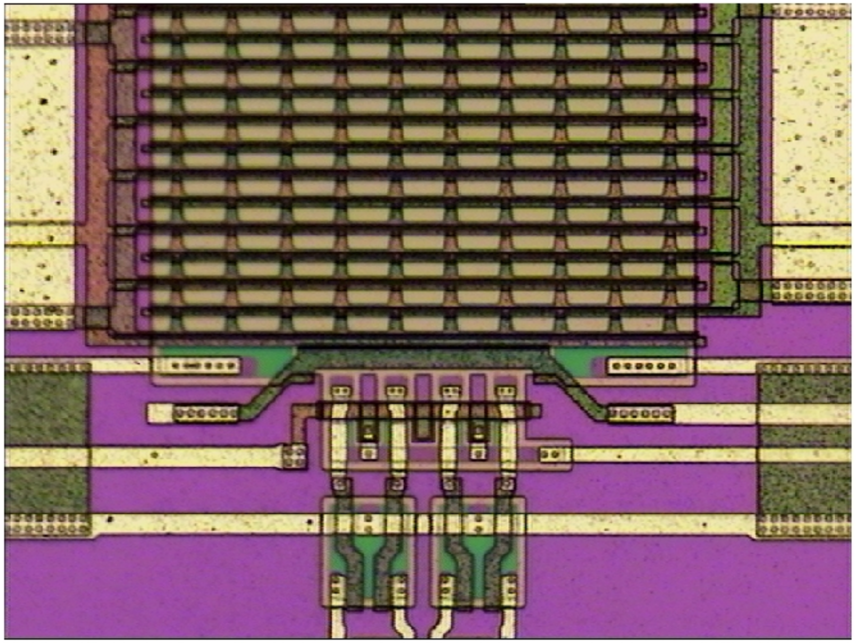


CCDs for Lower Gate Capacitance

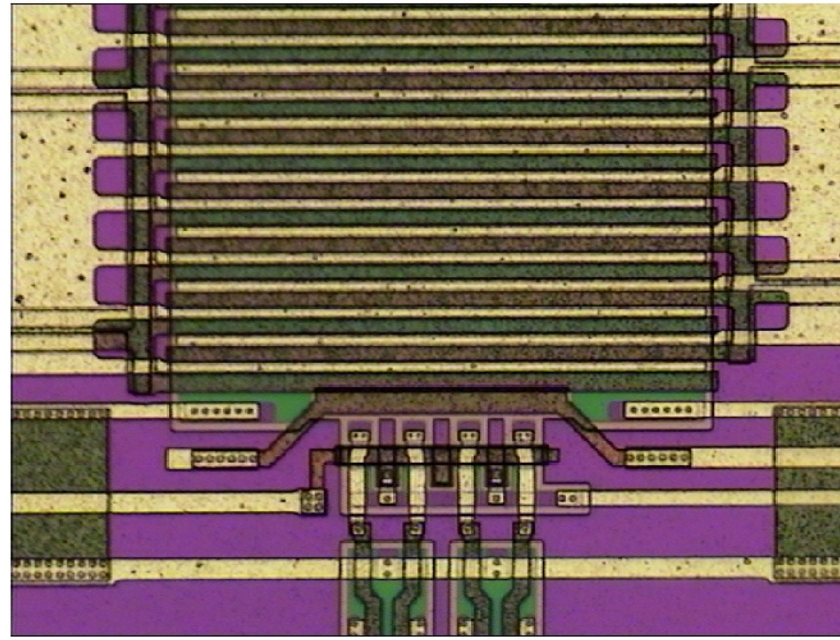


- Together with e2V Technologies designed 29 different types of small CCDs to test ideas
- 6-inch wafers now, CPC1 and CPC2 were on 5-inch
- 360 chips/wafer

CCDs for Lower Gate Capacitance



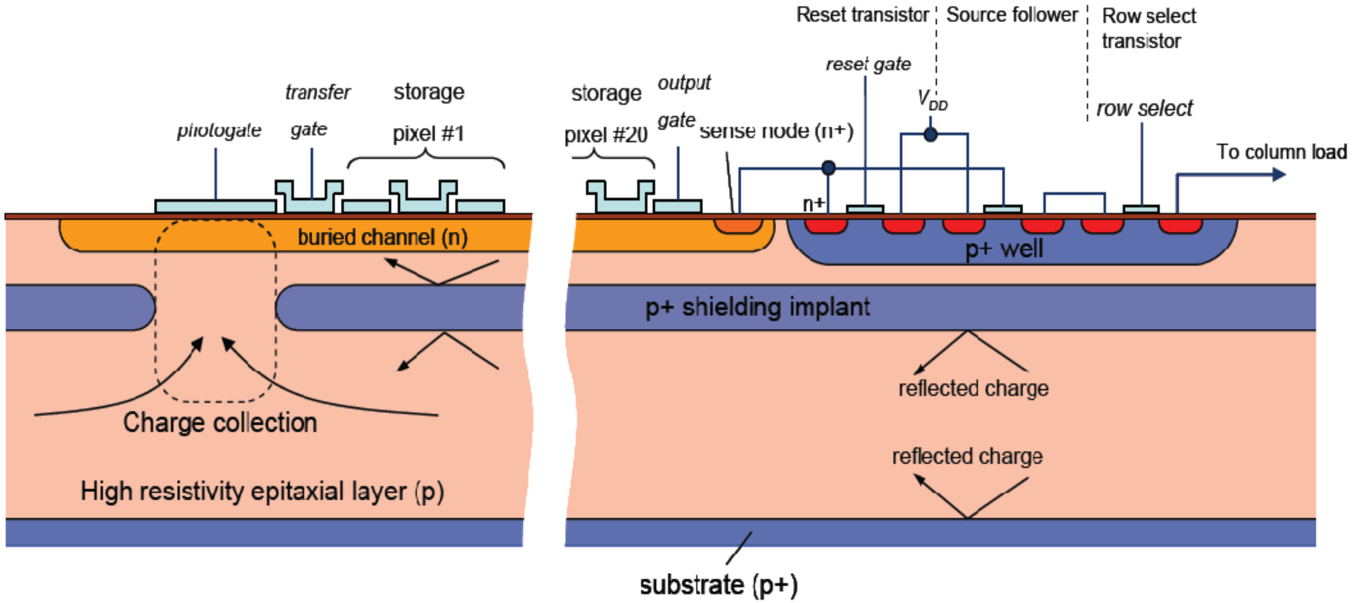
Open gate CCD



"Pedestal gate" CCD

- Two-stage source followers on 4 columns
- Lots of designs and process variants
- 4-phase drive with options for 2-phase

In-situ Storage Image Sensor (ISIS)

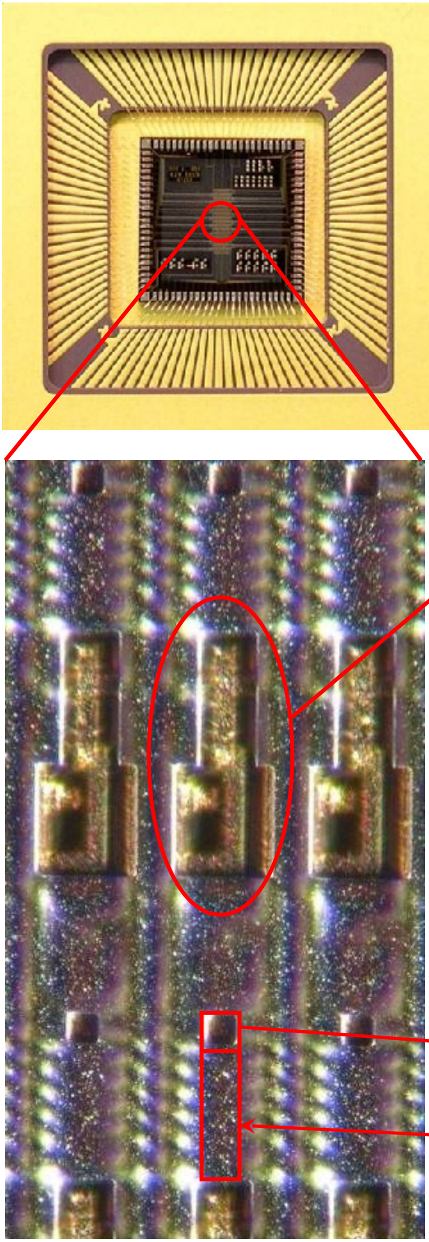


Operating principles of the ISIS:

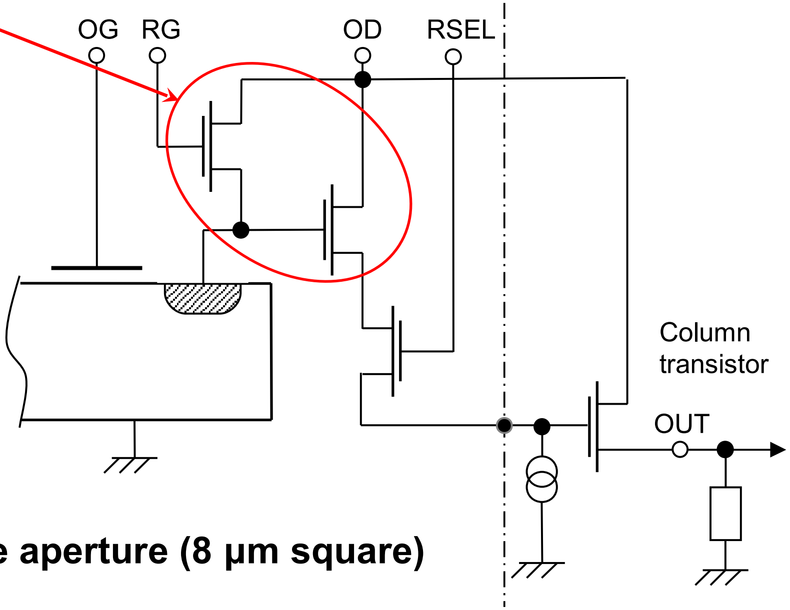
1. **Charge collected under a photogate;**
2. **Charge is transferred to 20-pixel storage CCD *in situ*, 20 times during the 1 ms-long train;**
3. **Conversion to voltage and readout in the 200 ms-long quiet period after the train (high tolerance to beam-related RF interference);**
4. **1 MHz column-parallel readout is sufficient;**

First ISIS Prototype : ISIS1

- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each;
- Cell pitch 40 μm × 160 μm, no edge logic (pure CCD process)
- Chip size ≈ 6.5 mm × 6.5 mm
- Manufactured by e2V Technologies (UK)



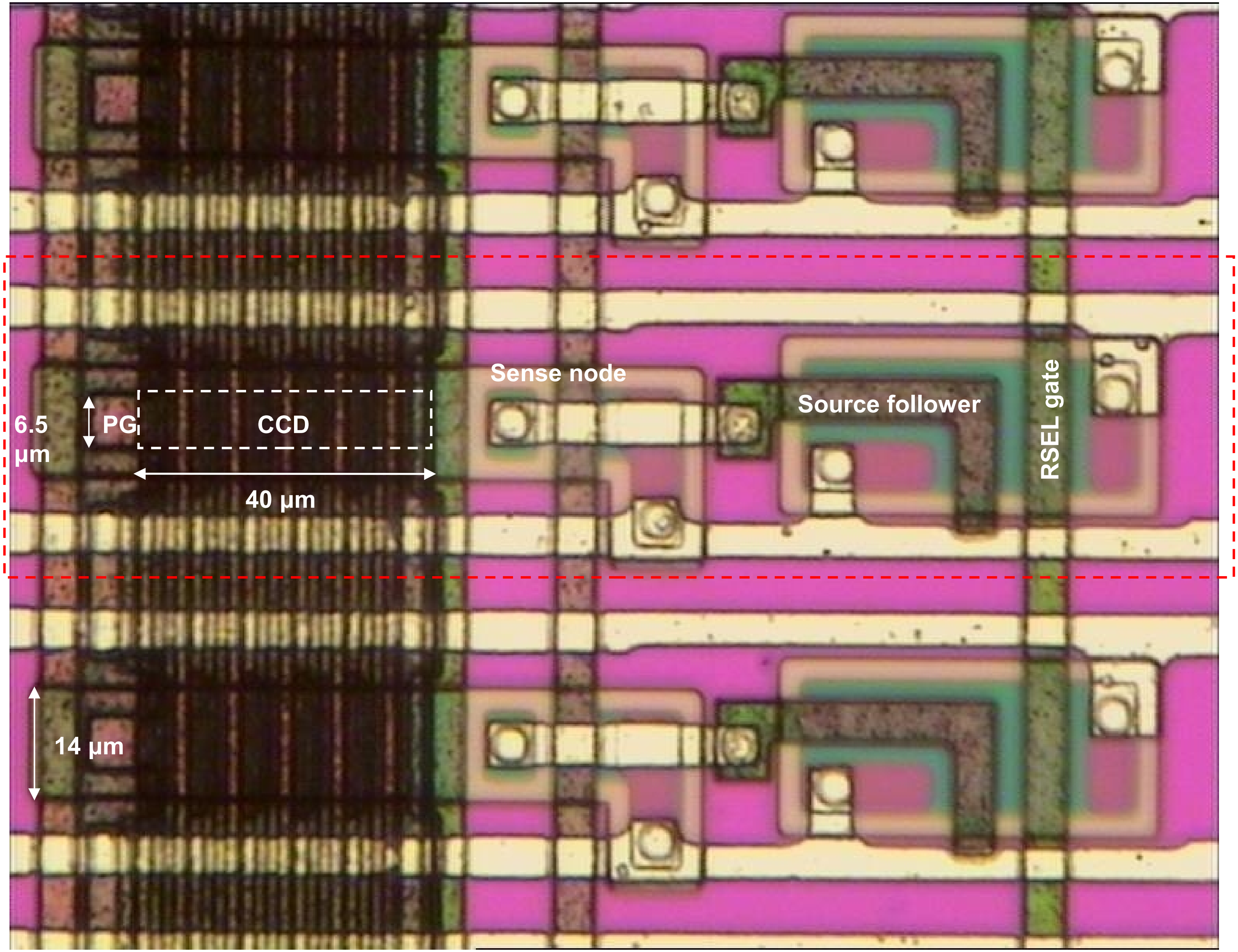
Output and reset transistors



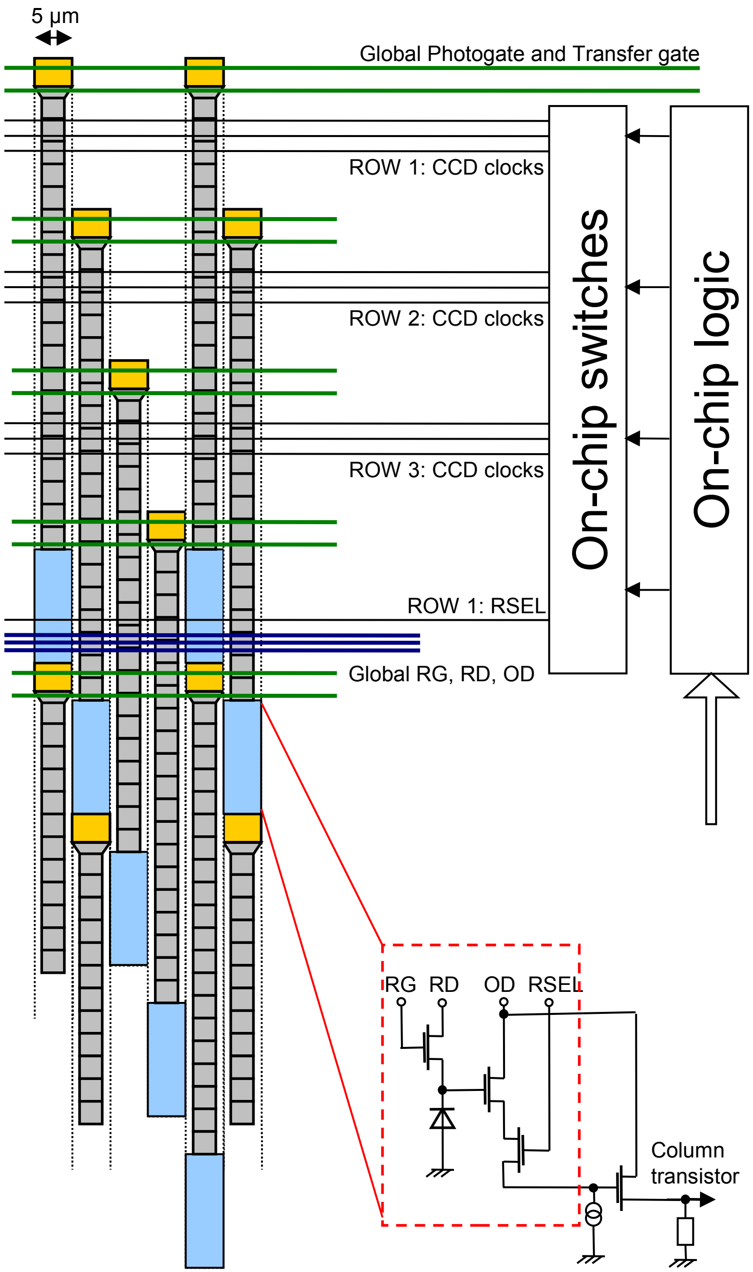
Photogate aperture (8 μm square)

CCD (5×6.75 μm pixels)

ISIS1 under the microscope

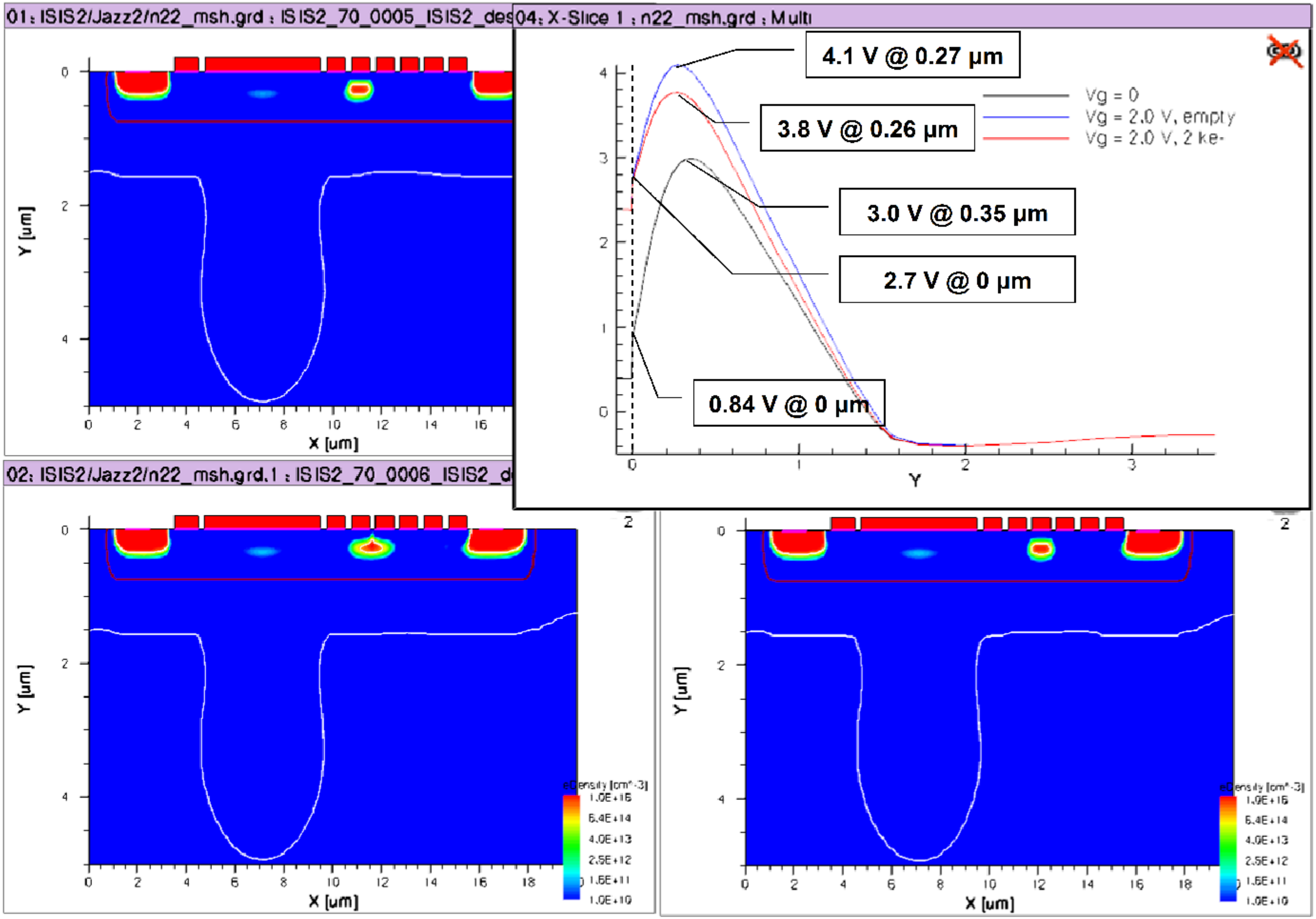


In-situ Storage Image Sensor (ISIS)



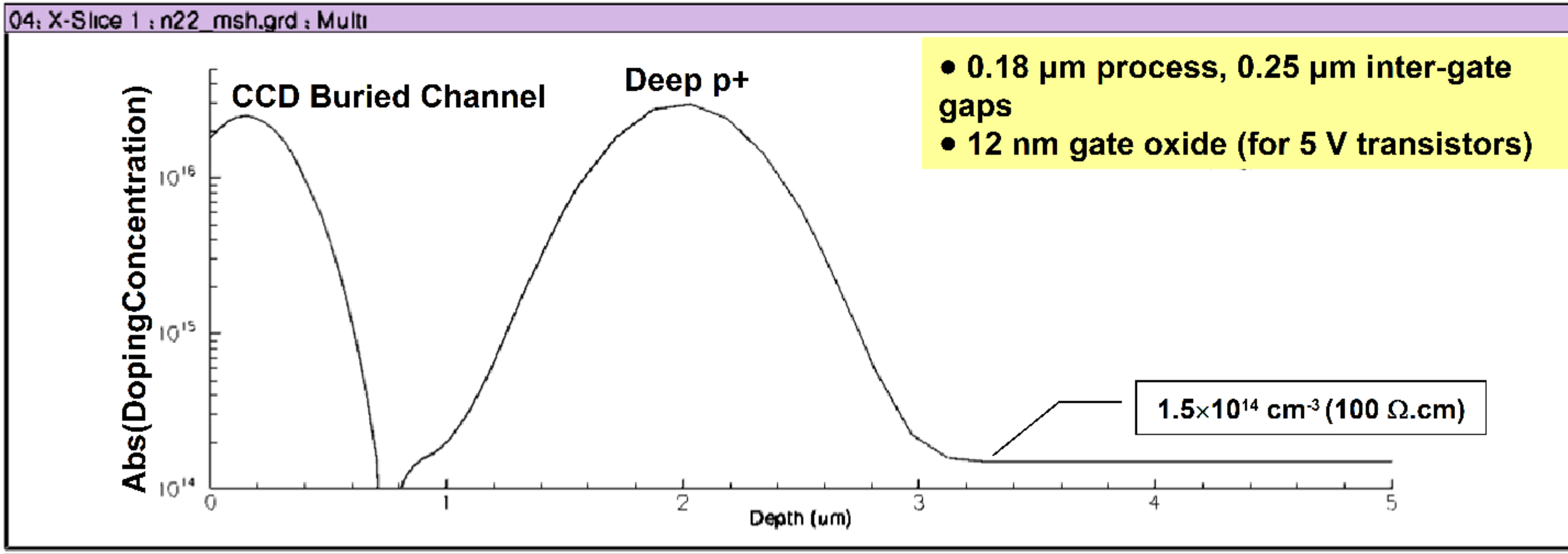
- The ISIS offers significant advantages:
  - Easy to drive because of the low clock frequency: 20 kHz during capture, 1 MHz during readout
  - ~100 times more radiation hard than CCDs (fewer charge transfers)
  - Very robust to beam-induced RF pickup
- ISIS combines CCDs, active pixel transistors and edge electronics in one device

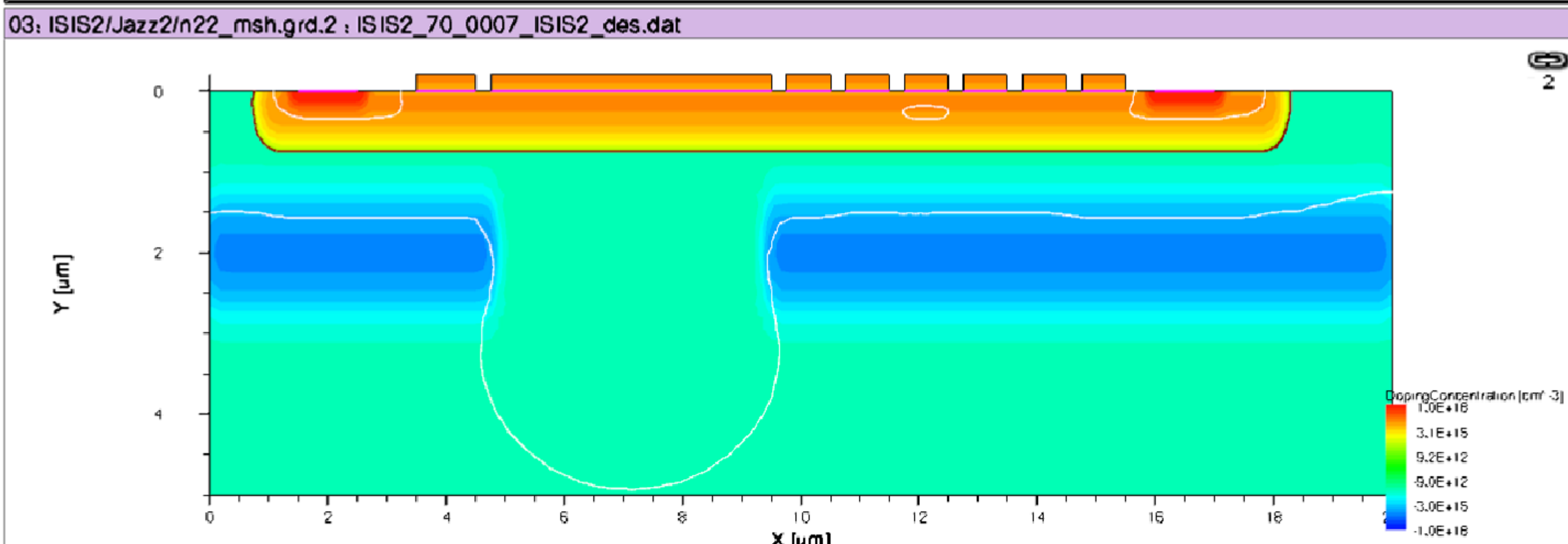
CMOS ISIS2 – Potentials

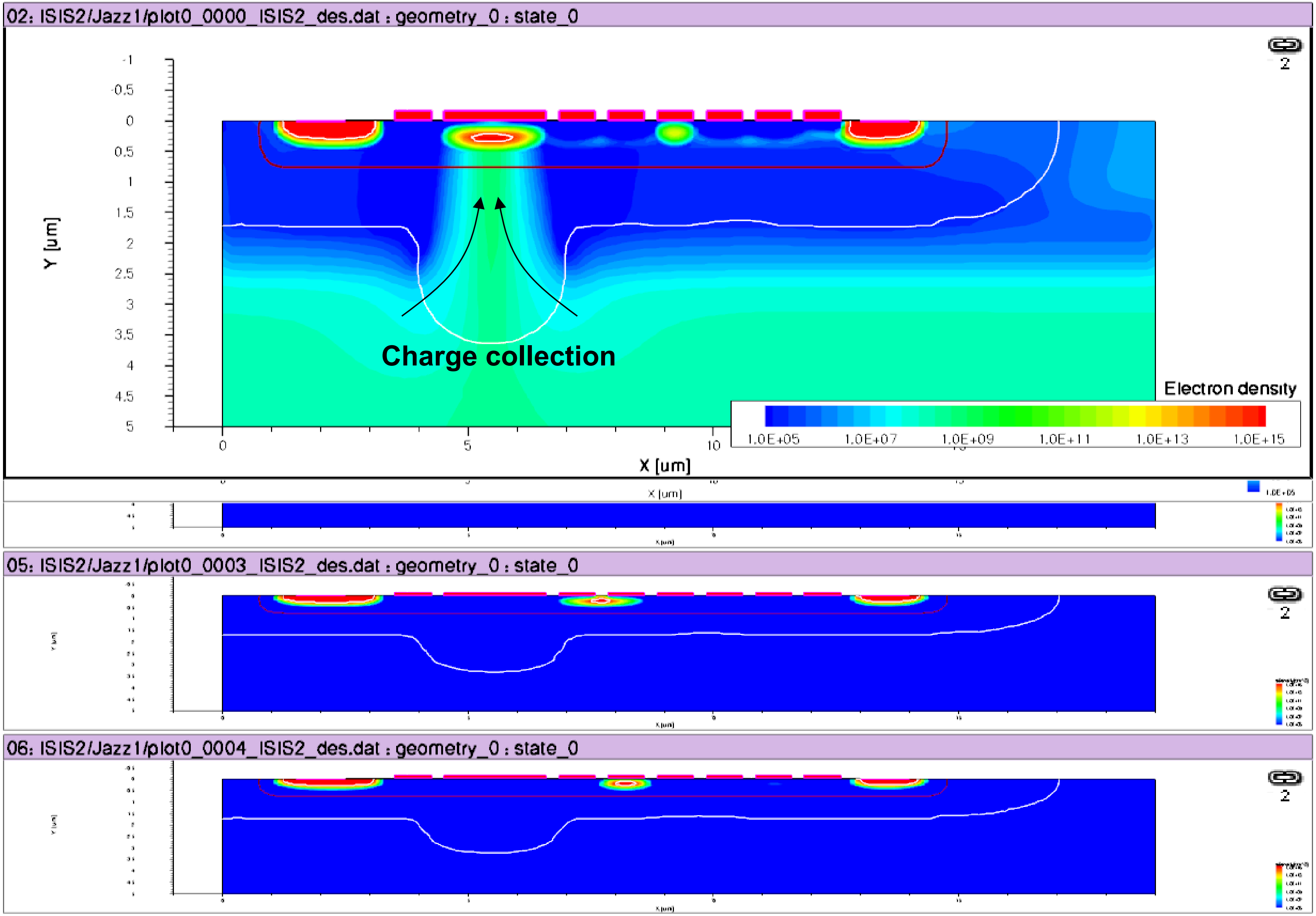


CMOS ISIS2 – Doping Profiles

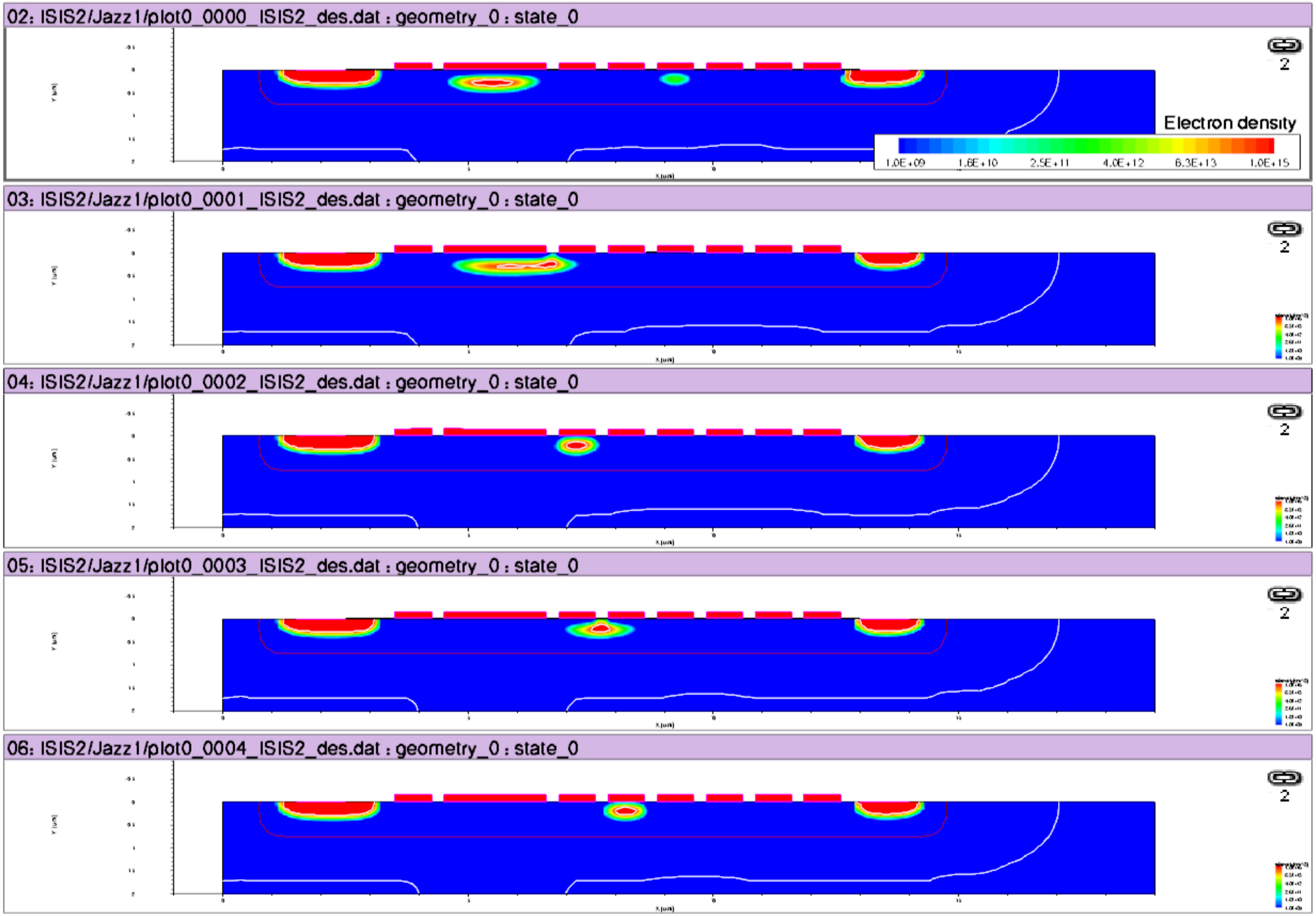
- 0.18 μm process, 0.25 μm inter-gate gaps
- 12 nm gate oxide (for 5 V transistors)



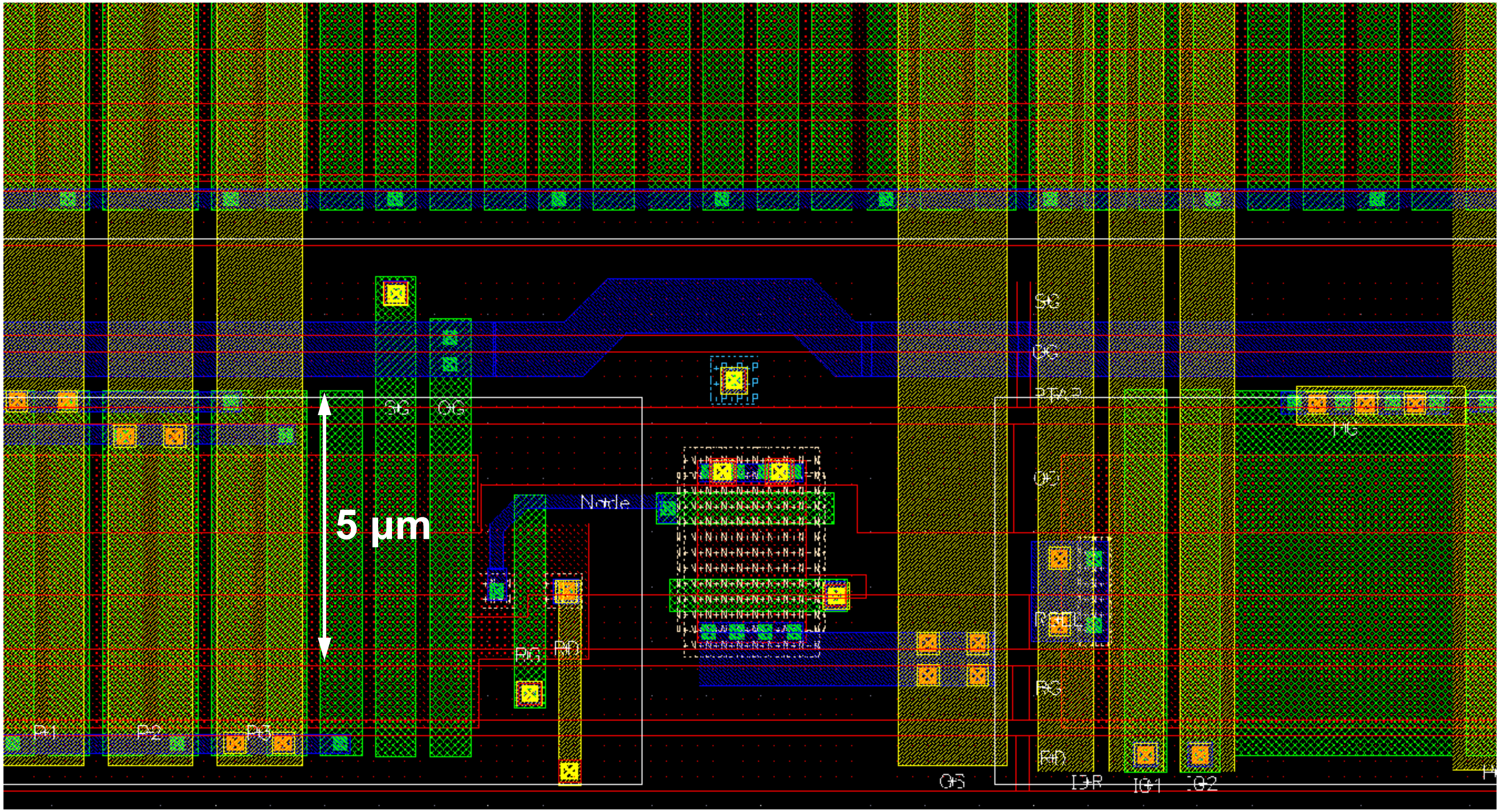



02: ISIS2/Jazz1/plot0_0000_ISIS2_des.dat : geometry_0 : state_0
Charge collection
Electron density
1.0E+05
1.0E+07
1.0E+09
1.0E+11
1.0E+13
1.0E+15
Y [um]
X [um]
05: ISIS2/Jazz1/plot0_0003_ISIS2_des.dat : geometry_0 : state_0
06: ISIS2/Jazz1/plot0_0004_ISIS2_des.dat : geometry_0 : state_0

CMOS ISIS2 – Charge Transfer

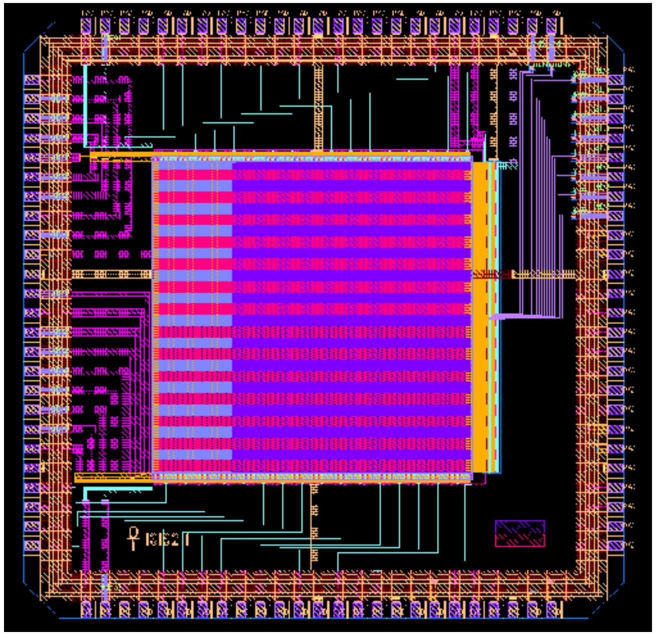


ISIS2 – Pre-release Pixel Layout



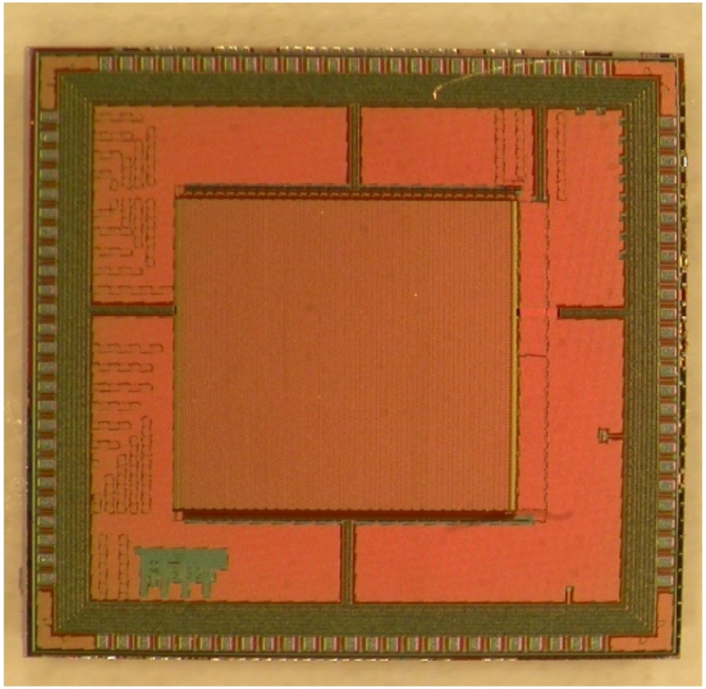
- 80 µm × 10 µm pixels
- 5 µm wide buried channel, 3+3 metal layers

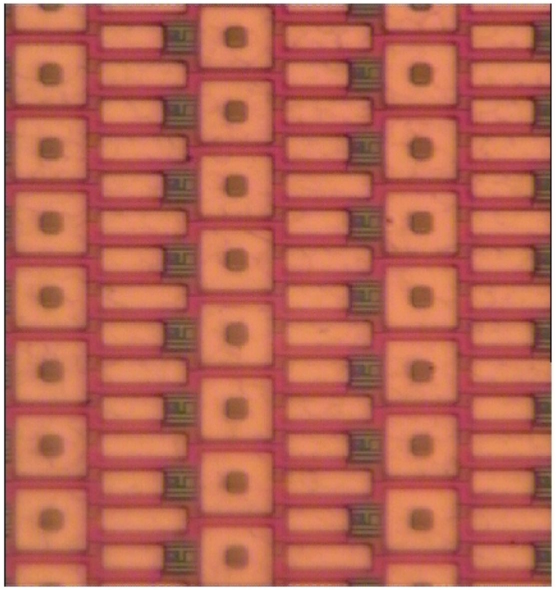
ISIS2 – Summary



- One of the first monolithic buried channel CCD/CMOS devices in the world
  - Several different pixels designs
  - Many test structures
- Design derived after intensive simulation work
- Custom doping profiles
- Non-overlapping, single layer polysilicon gates
- Deep p+ buried implant for charge shielding
- Buried channel and surface channel transistors
- Made on a customised 0.18 μm 6-level metal dual gate (1.8V/5V) imaging CMOS process

ISIS2 – Results





Results:

- Device works well, but new untested technology has produced some surprises
- Charge transfer demonstrated
- Noise around 5 e- rms
- Storage pixel capacity = 6ke-

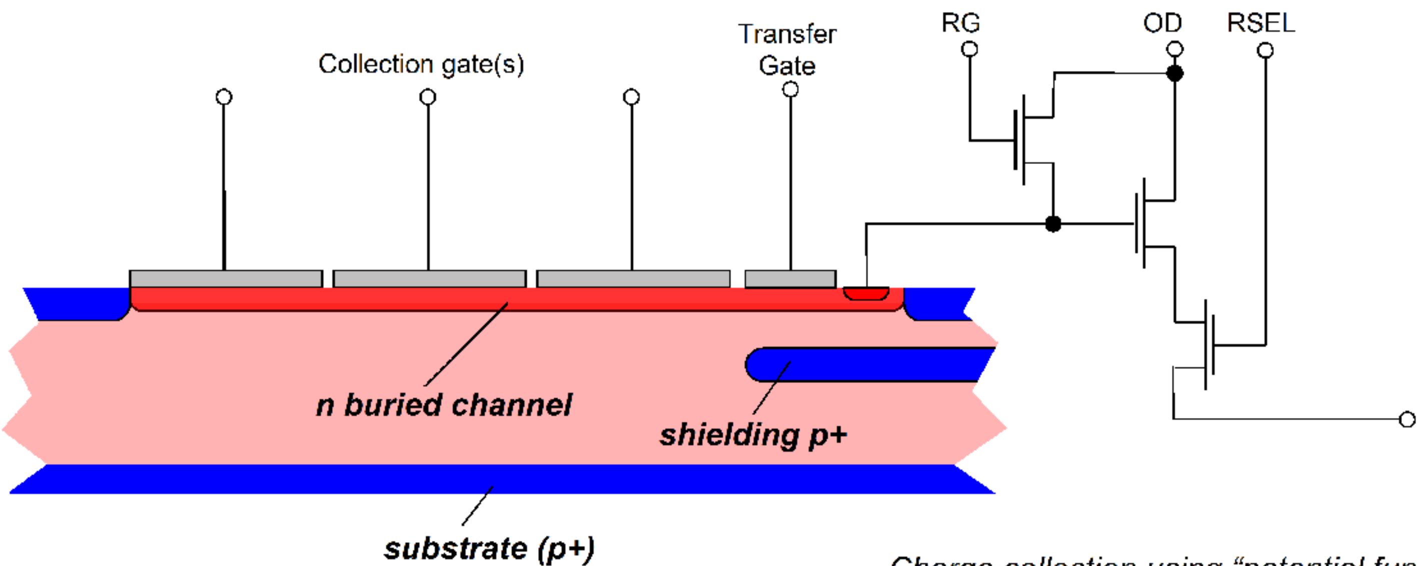
Charge Transfer in CMOS

Why charge transfer in CMOS?

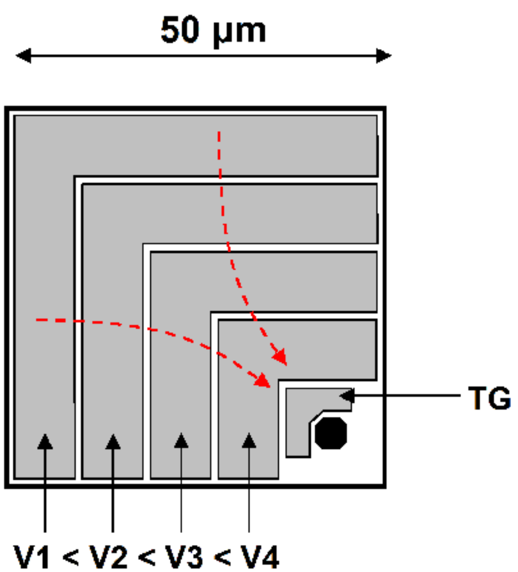
- **Allows separate optimisation of charge collection and charge sensing elements**
  - **Large pixels with fast charge collection in CMOS possible**
  - **High responsivity due to the low capacitance sense node in sub-micron CMOS**
  - **Sophisticated on-chip logic and electronics**
- **Allows signal processing of charge without adding electronics noise**
- **Opens up new opportunities in CMOS:**
  - **Time delayed integration**
  - **Electron multiplication by impact ionisation**
  - **Completely new applications**
- **Number of transfers should be kept low to avoid inefficiency.**

Other Applications for Tracking

Photogate transfer with Buried Channel CCD storage

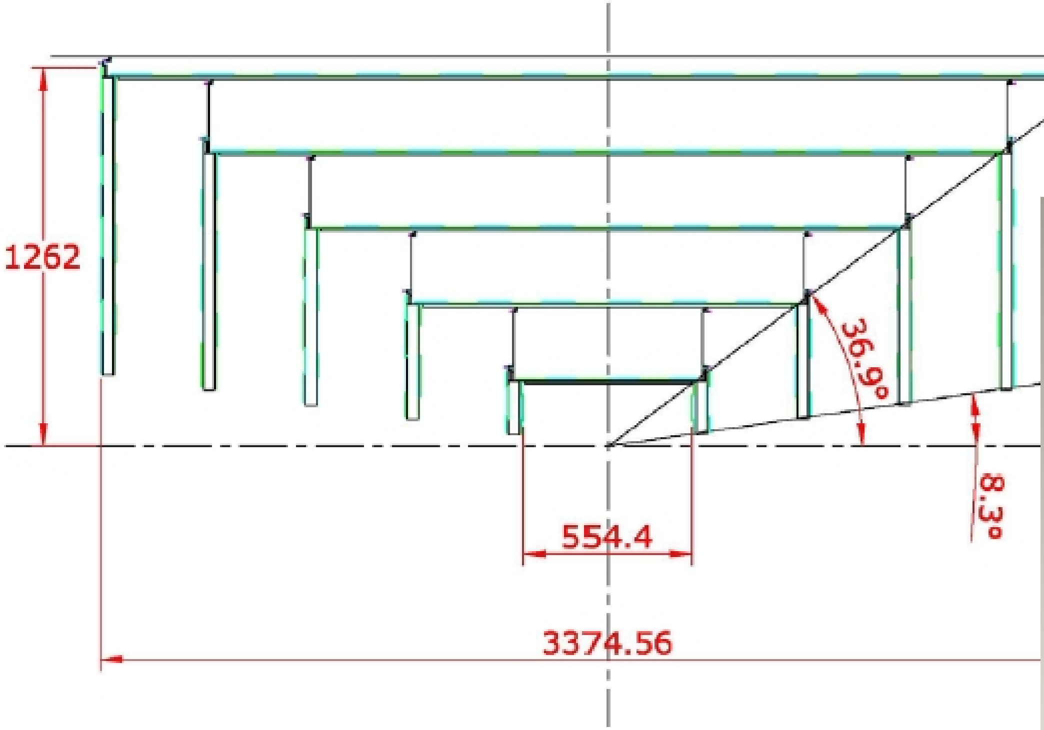


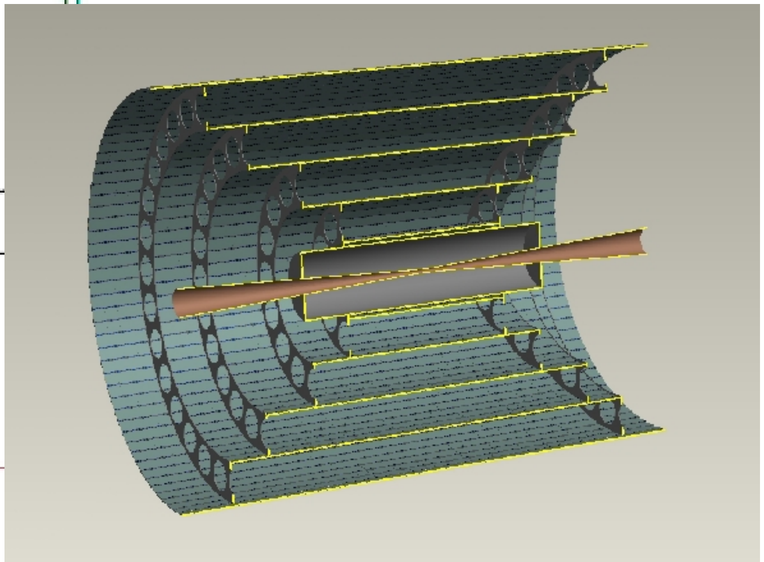
Charge collection using "potential funnel", inspired by Grzegorz Deptuch (Fermilab)



- Large pixels thanks to buried channel collection
- Charge collection is faster due to larger depleted areas
- Charge transfer allows optimal correlated double sampling and low noise
- Charge transfer to the node by "funnel" action
- Possible problems with inefficient transfer due to inter-gate gaps

Silicon Pixel Tracker Based on the SiD Design

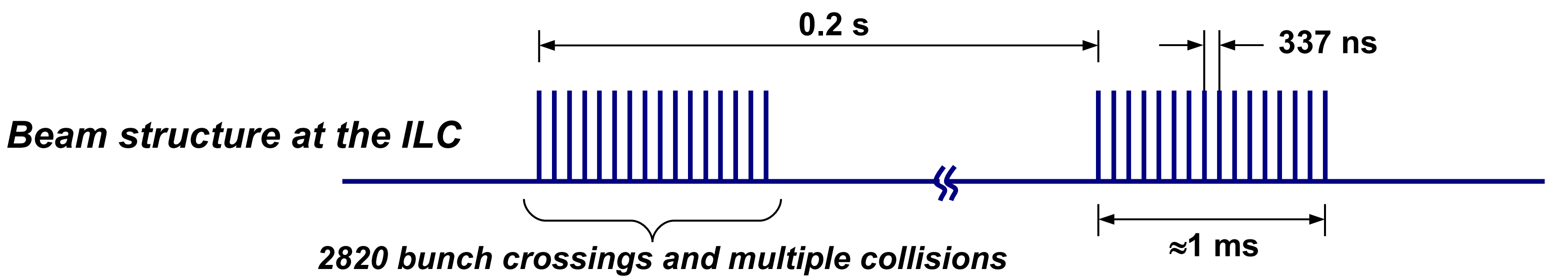


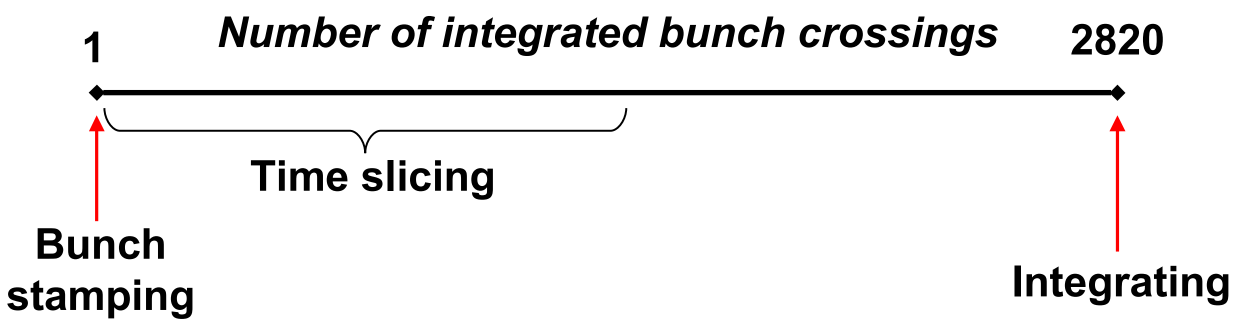


Silicon Pixel Tracker for ILC:

- Barrel and Forward trackers, total area = 70.3 m^2
- With 50 μm × 50 μm pixels – 28.1 Gpix system
- Low mass support, gas cooling
- If each chip is 8 cm × 8 cm (2.6 Mpix): 11,000 sensors is total
- Readout and sparsification scheme to be developed

Integrating, Time Slicing, Bunch Stamping Options





<u>In the barrel:</u>

- **It could be possible to integrate all events (and the background) and read in the inter-train gap**
- **It remains to be proven that the pattern recognition does not deteriorate**
  - **Additionally, the detector becomes highly tolerant to beam-induced EMI**

General Considerations for the SPT

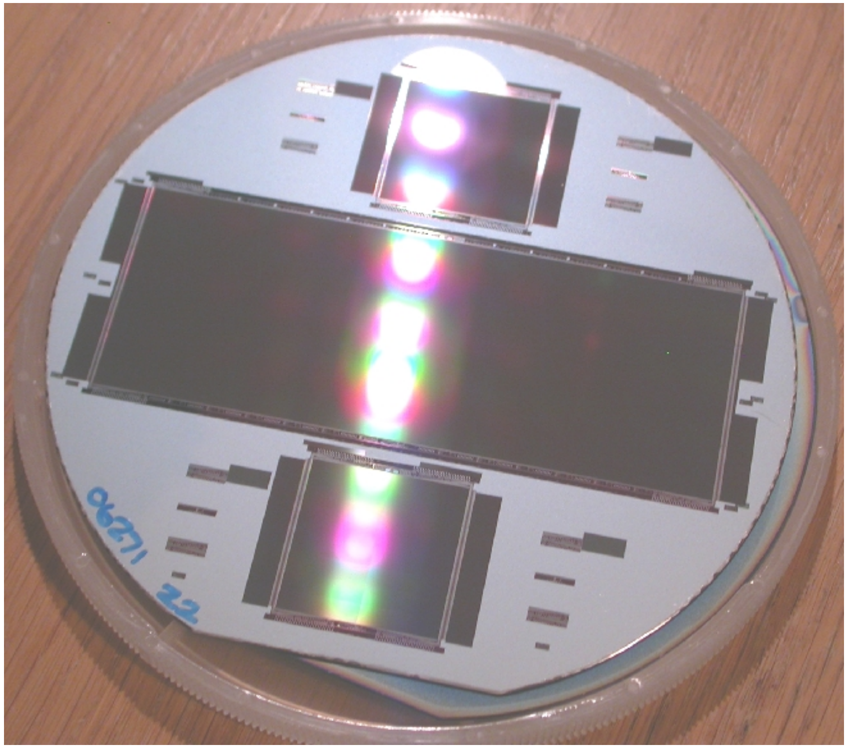
- The main challenge is to reduce material and therefore power
- Sensors ≈100 μm thick, low mass support (<1% X_0 per layer in the SiD design)
- Gas cooled, power dissipation ~O(100 W), in SiD < 500 W
- Pixel size around 50 μm × 50 μm (point resolution ≈14 μm in binary mode)

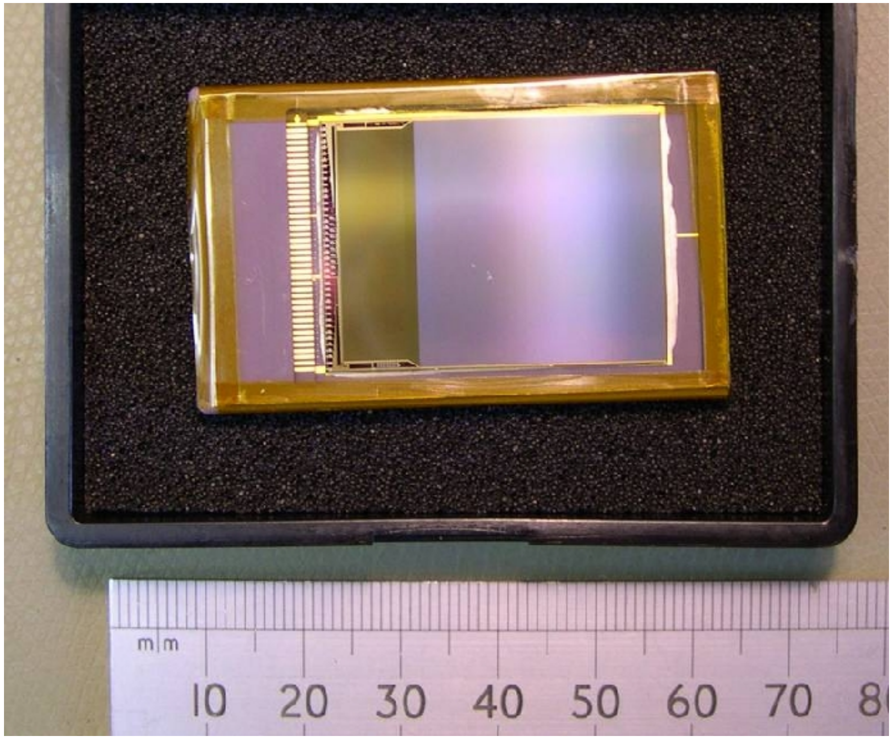
- Bunch stamping/time slicing tracker:
  - Implies on-pixel intelligence and therefore more power
  - Binary readout and sparsification most likely, but measurement of charge centroid is not excluded
- Integrating:
  - Lowest power (due to slow readout) and low mass
  - Full pixel readout to local readout chip
  - Resolution likely to improve below 14 μm due to the use of charge centroid

<u>We have considered two technology solutions:</u>

- Charge Coupled Devices – can do only integrating
- Monolithic Active Pixel Sensors – can do bunch stamping, time slicing, integrating

Large Existing CCDs

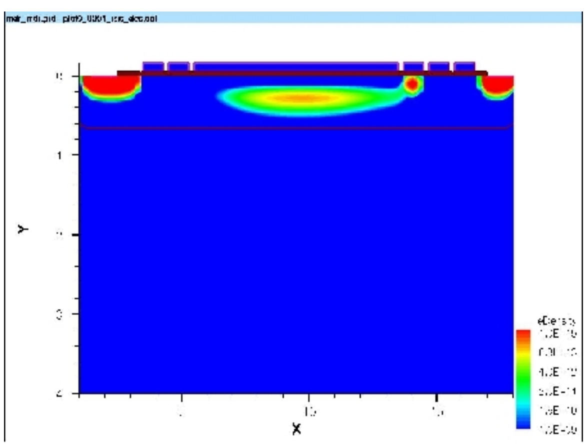


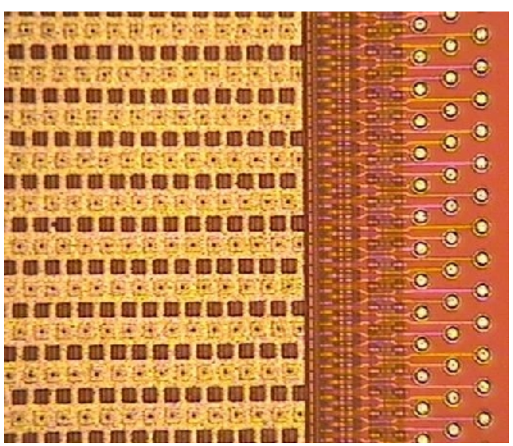


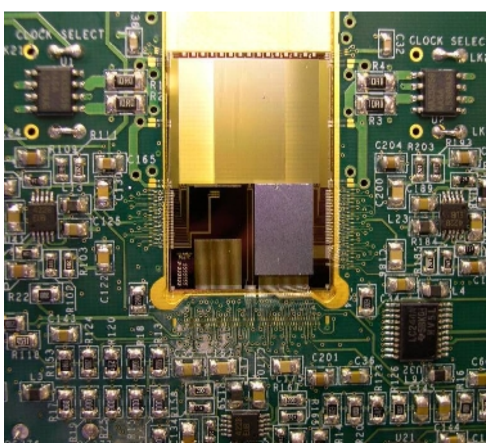
- Wafer scale CCD from e2V
- 6-inch wafers

- 40 µm pixel CCDs using advanced charge collection and transport
- Noise = 5e- at 1 MHz
- Samples from e2V

- **CCD-based detectors for particle physics offer unique advantages**
- **CPCCD : Complex high speed hybrid assemblies with 2 ASICs demonstrated**
- **ISIS : novel CMOS sensor with CCD signal storage**
- **Bright future ahead for advanced CCD/CMOS imaging devices**
  - **Combining the best of both worlds**
  - **Open up new applications**
  - **First devices made, more to be done**

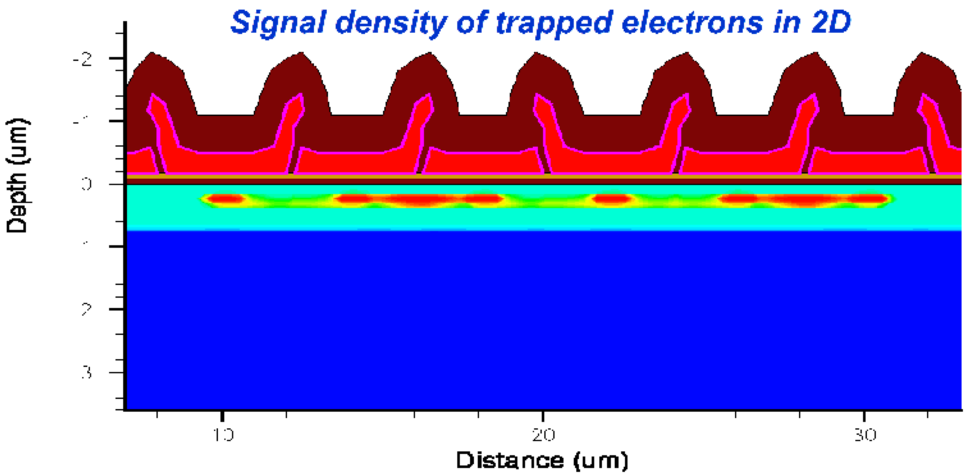


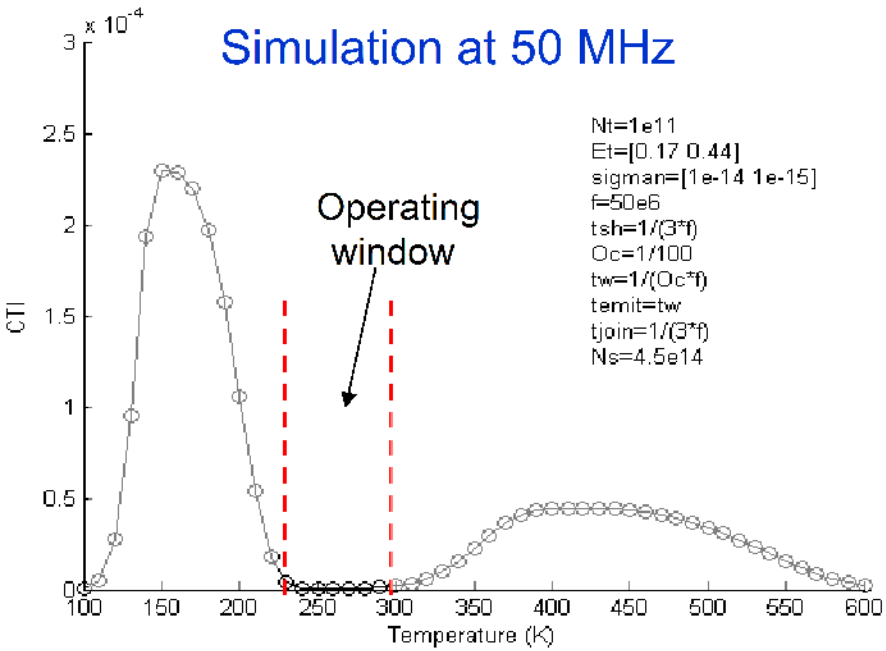




Additional Material

Radiation Damage Effects in CCDs: Simulations

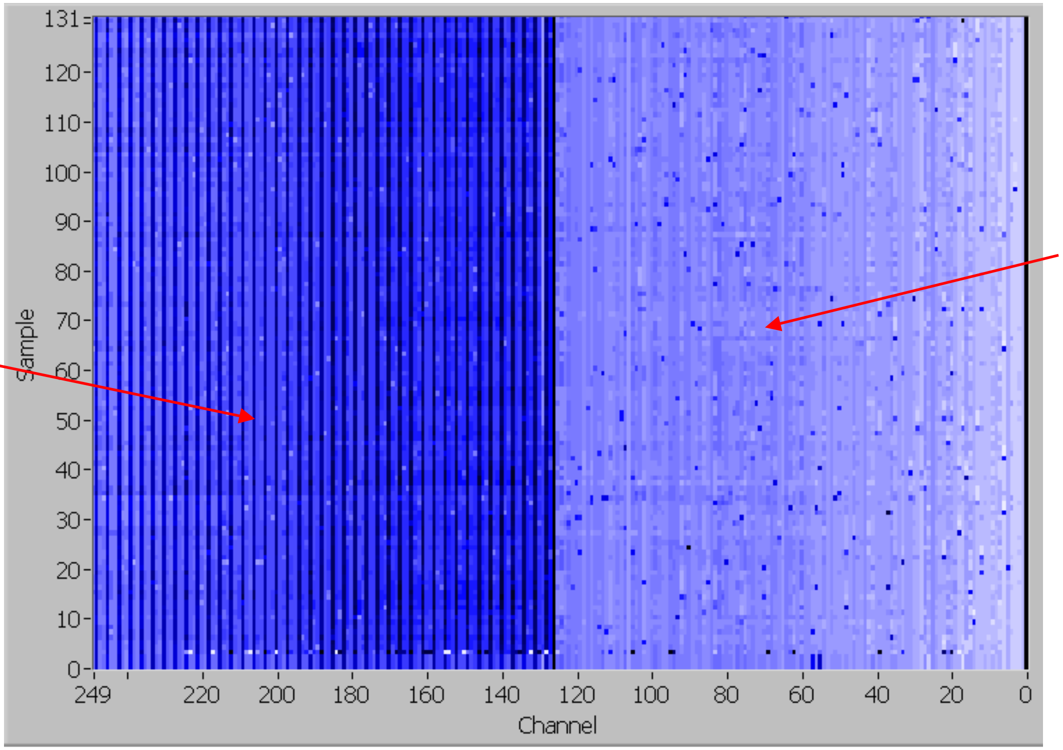




- Full 2D simulation based on ISE-TCAD developed
- Trapped signal electrons can be counted
- CPU-intensive and time consuming
- Simpler analytical model also used, compares well with the full simulation
- Window of low Charge Transfer Inefficiency (CTI) between -50 °C and 0 °C
- This is very important for the viability of the CCD option and should be verified experimentally

CPC1/CPR1 Performance

5.9 keV X-ray hits, 1 MHz column-parallel readout



Charge outputs, inverting (positive signals)

Noise ≈100 e-

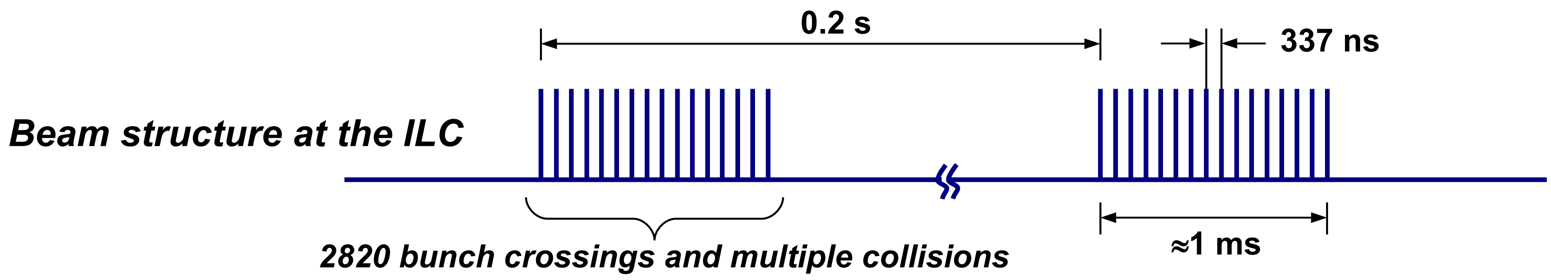
Voltage outputs, non-inverting (negative signals)

Noise ≈60 e-

- **First time e2V CCDs have been bump-bonded**
- **High quality bumps, but assembly yield only 30% : mechanical damage during compression suspected**
- **Differential non-linearity in ADCs (100 mV full scale) : addressed in CPR2**

Bump bonds on CPC1 under microscope

Beam Structure at the ILC and Implications for the Tracker



Considering the barrel:

- **Physics event rate is tiny: 1.5 hits/BX over all of layer 1 (20 cm radius)**
- **Background is photons:**
  - **Converted on 300 μm Si gives 0.002 hits/cm^2.BX, or 6 hits/cm^2 for the train (in the barrel)**
  - **On 100 μm thick Si this is 2 hits/cm^2 for the train**
- **With 50 μm × 50 μm pixels (point resolution ≈14 μm) the occupancy in L1 would be only 0.005% for the whole bunch train!**